UBM Electronics

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VOICE OF THE ENGINEER

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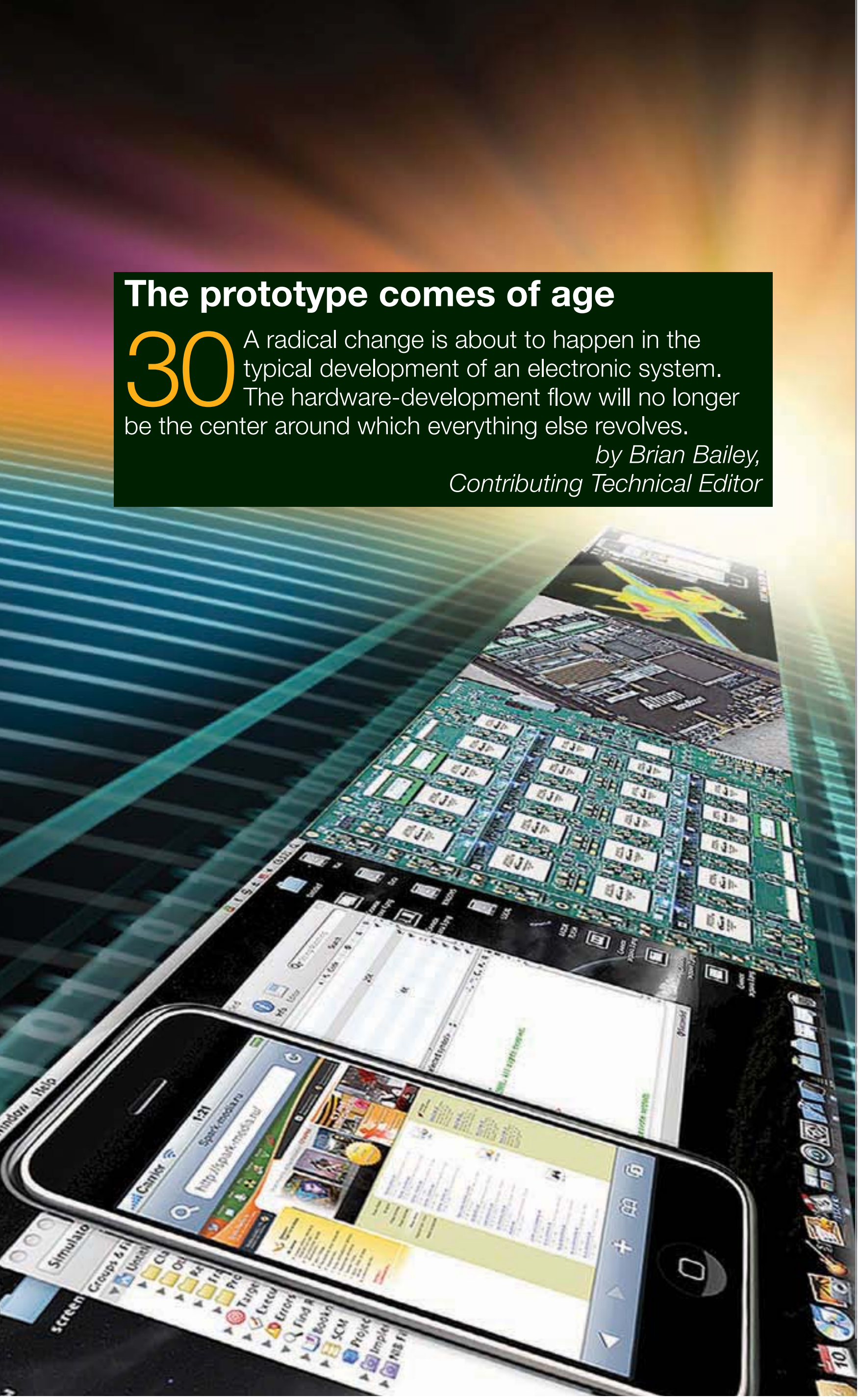

The prototype comes of age

30 A radical change is about to happen in the typical development of an electronic system. The hardware-development flow will no longer be the center around which everything else revolves.

by Brian Bailey, Contributing Technical Editor

IMAGE(S): SHUTTERSTOCK

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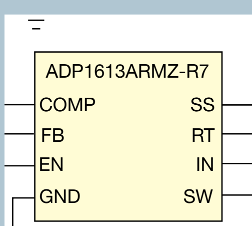

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▶ Find out how to submit your own Design Idea: http://bit.ly/DesignIdeasGuide.


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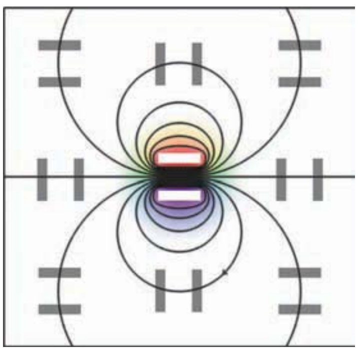

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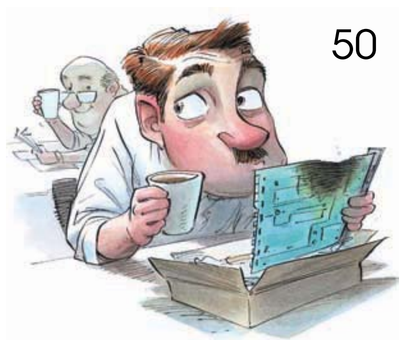

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EDN® (ISSN# 0012-7515) is published semimonthly by UBM Electronics, 600 Community Drive, Manhasset, NY 11030-3825. Periodicals postage paid at Manhasset, NY, and at additional mailing offices. SUBSCRIPTIONS—Free to qualified subscribers as defined on the subscription card. Rates for nonqualified subscriptions, including all issues: US, $150 one year; $250 two years; $300 three years. Except for special issues where price changes are indicated, single copies are available for $10 US and $15 foreign. For telephone inquiries regarding subscriptions, call 847-559-7597. E-mail: edn@omeda.com. CHANGE OF ADDRESS—Notices should be sent promptly to EDN, PO Box 3609, Northbrook, IL 60065-3257. Please provide old mailing label as well as new address. Allow two months for change. NOTICE—Every precaution is taken to ensure accuracy of content; however, the publishers cannot accept responsibility for the correctness of the information supplied or advertised or for any opinion expressed herein. POSTMASTER—Send address changes to EDN, PO Box 47461, Plymouth, MN 55447. CANADA POST: Publications Mail Agreement 40612608. Return undeliverable Canadian addresses to BleuChip International, PO Box 25542, London, ON N6C 6B2.

Volume 57, Number 1 (Printed in USA).

EDN online

JOIN THE CONVERSATION

Comments, thoughts, and opinions shared by *EDN*'s community

In response to "Solyndra: Its technology and why it failed," by Don Scansen of IP Research Group, http://bit.ly/s86np1, Robert Cox, a design engineer in Tampa, FL, comments:

"Solyndra's technology was good, but it was the installation that was brilliant. In Florida, where storm events drive the cost of panel installations on commercial roofs requiring through-bolt installations, the Solyndra system would have been ideal and would have made up for module cost in installation savings. Unfortunately, the Florida legislative structure favors utilities and prevents the adoption of solar power ... . Unfortunately for Solyndra, our time did not come to save this innovative product. We hope our legislators do wake up."

In response to "The sun will screw up tomorrow," a Tales from the Cube column by Clark S Robbins, http://bit.ly/u35Z6s, William Ketel, an engineer in Michigan, comments:

"I am attempting to imagine what sort of organization would assert that a nonreproducible failure was not fixable and so could not be repaired. The process that has often been used in such cases is usually termed the shotgun approach and consists of replacing all of the parts of the system, including those pieces that 'cannot fail.' This method is seldom cheap, but, in many cases, ... it is cost-effective. But I do wonder why anyone would assume that a connector could not fail. ... Connectors have a great many potential failure modes, most of which are intermittent and seldom reproducible."

EDN *invites all of its readers to constructively and creatively comment on our content. You'll find the opportunity to do so at the bottom of each article and blog post. To review current comment threads on EDN.com, visit http://bit.ly/EDN_Talkback.*

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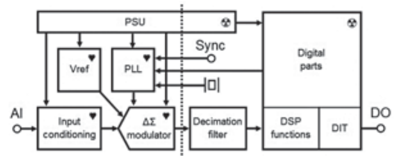
Can't-miss content on EDN.com



AUDIO-CONVERTER-SUBSYSTEM DESIGN CHALLENGES IN THE 21ST CENTURY

Most audio-converter subsystems perform below the potential of their chosen data converter. Ian Dennis of Prism Sound examines why that situation might be and offers tips on how to achieve optimum audio-converter performance.

http://bit.ly/w29NCL

TOSHIBA'S ECO CHIP ENABLES LCD TV'S 0W STANDBY MODE

Perception of "greenness" can be a marketing advantage in consumer devices. Toshiba's 32-in. flat-screen LED-backlit LCD TV, the Regza 32BE3, achieves 0W standby power with the Eco Chip. Meanwhile, many readers comment that it would be even greener to not waste time watching TV.

http://bit.ly/sw5WPp

ENGINEERING COMMUNITY

Opportunities to get involved and show your smarts

***EDN*'s VOICE OF THE ENGINEER BLOG** is all about giving you, the engineer, a voice. Open to our audience, we encourage engineers to share their perspectives on all matters of engineering, be that what's happening in the electronics industry, changes to design, what it means to be an engineer, or anything else of relevance to you and your peers. E-mail submissions to edn.editor@ubm.com and tune in to see what your fellow EEs have to say.
http://bit.ly/VoiceOfTheEngineer

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BY SUZANNE DEFFREE, MANAGING EDITOR, ONLINE

Get off the sidelines

Progress: It's what engineers do. They advance, they grow, and they move forward. To engineers, there is nothing more defeating than standing still or, worse, taking a step back. Yet, for many engineers, 2011 was a year of maintenance or recovery following a layoff or budget cuts. Read the Voices question-and-answer column in our last issue, and it's easy to see why (**Reference 1**). For that column, Bill McClean, president of market-research company IC Insights, spoke to *EDN* about 2011's less-than-expected semiconductor-industry growth, estimates for 2012, and why the always-complex semiconductor market cannot be judged on just one of its aspects. McClean graciously gave *EDN* 30 minutes of his time for the interview, and, in that half-hour, he made several wise points based on his more than 30 years of experience tracking the IC industry.

IMAGE: ISTOCKPHOTO

One point really hit home for me: "We've always said that uncertainty is the worst thing in the marketplace," McClean said. "It's actually worse than bad news. If you know something is going to be bad, you can plan around it. But uncertainty creates total fear and total apprehension, and it makes people freeze. They don't do anything; they just sit on the sidelines. 2011 saw a tremendous amount of uncertainty, and that [feeling] showed up in the semiconductor market."

Look below the surface of this month's quarterly reports and cheerful toasts from execs at your company holiday parties just a few weeks ago, and you'll see that a conspicuous—and understandable—amount of fear remains in this industry. After all, 2011 was supposed to be the year of double-digit growth, the return to gains, and the "normalizing" after years of disorder.

Invest time and resources in smart ideas that have potential, not just established product lines.

Instead, we saw tsunamis, floods, and earthquakes disrupt some lives, supply chains, and purchasing habits. Add in the high unemployment rate in the United States, the economic confusion in Europe, the deaths of some of the industry's greatest engineers, and the re-emergence—or continuation—of R&D tightening, and you'll realize that not many in this industry will fondly remember 2011.

It's now time to move past those woes, however. No one can say for sure that 2012 will be clear of problems. But we *can* state that it's no longer 2008, 2009, or 2010, and we've closed 2011. It's time to get off the sidelines and charge forward. Leave the last four years of turmoil behind and move ahead, away from the fear.

We have no control over plenty of things, including natural disasters, death, or the worldwide GDP, but there are things that we—or, perhaps, our managers—can do to get off the sidelines and make progress. Number 1 on that list should be hiring the best people available. Companies don't grow without talented people, and they don't grow by overworking the talented people already on staff. Number 2: Take some risks again. Invest time and resources in smart ideas that have potential, not just established product lines. Number 3: Prepare to get knocked down. It's going to happen. No matter how well you innovate and plan, you will at some point be tackled unexpectedly if you get off the sidelines and into the game. You can bet that the guys heading to Indianapolis in a few weeks got hit a lot on their way to the Super Bowl. So keep your helmet handy and proceed aggressively but defensively.

We start a new year this week. As the hangover of 2011 subsides, plan your 2012 with progress in mind. Make it—not maintenance—a priority. Get off the sidelines and back into the game. **EDN**

REFERENCE

1 Deffree, Suzanne, "Bill McClean: Don't broad-brush the semiconductor market," *EDN*, Dec 15, 2011, pg 22, http://bit.ly/w0fTm8.

Contact me at suzanne.deffree@ubm.com, or go to http://bit.ly/sO0XUF to post a comment on this column.

pulse

INNOVATIONS & INNOVATORS

Precision dual sensor op amp features high voltage, low noise, near-zero drift

Forget about the converter or software for now: A good sensor signal chain starts with a good front-end op amp. The Maxim MAX44251 dual device is the latest op amp to strive for nearly ideal performance, along with the higher supply-rail voltages that industrial-level applications require. It operates from a 2.7 to 27V supply and includes initial maximum offset lower than 6 μV, along with a proprietary autocorrelating, autozero calibration approach, which keeps maximum drift lower than 19 nV/°C over the –40 to +125°C range. Autozero offset calibration also eliminates the effects of power-supply and even common-mode variations.

Gain bandwidth is 10 MHz, and current consumption is 1.15 mA per channel. Input-referred noise is 5.9 nV/√Hz, which the vendor claims is the lowest available for a high-voltage, autozeroing component. Other critical specifications include PSSR, CMRR, and large-signal voltage gain of 135 dB at 25°C. The IC also offers RF immunity, which is critical in many industrial and medical installations in RF-heavy environments.

The MAX44251 is available in eight-lead SOT-23 and μMAX packages and sells for $1.48 (1000). **—by Bill Schweber**

▷**Maxim Integrated Products**, www.maxim-ic.com.

The MAX44251 dual sensor op amp targets use in precision-sensing applications.

TALKBACK

"There can be wisdom and value in holding onto some things that do not appear to be immediately useful. Unfortunately, there is an excess number of the opposite variety around—those who will trash every part not used in a project, including all of the standard parts that could go into stock."

—Electrical engineer and technical writer William Ketel, in *EDN's* Talkback section, at http://bit.ly/tbldhX. Add your comments.

Modular real-time DSOs hit 60 GHz on as many as 10 channels simultaneously

LeCroy has announced the LabMaster 10 Zi-A (LM10Zi-A), a large, modular scope that acquires 80G samples/sec/channel and can deliver 36-GHz bandwidth on four to 20 channels. Thanks to patented frequency-domain-based DBI (digital-bandwidth-interleaving) technology, it can acquire 160G samples/sec/active channel and deliver 60-GHz real-time bandwidth on two to 10 channels. Bandwidth greater than 33 GHz has previously been available only from sequential equivalent-time-sampling scopes, which, though accurate, don't well suit many multigigahertz-scope measurements that signal-integrity engineers and high-speed-optical-communication-network designers make.

The LabMaster 10 Zi-A system acquires as many as 10 60-GHz-bandwidth signals simultaneously—many more signals with greater bandwidth and significantly higher sampling rate than are possible with any other real-time digital scope.

The company adopted the modular approach for several reasons. For example, few probes have bandwidths greater than approximately 30 GHz. This lack often necessitates the use of pairs of channels as differential inputs for capturing signals that contain significant energy at frequencies of 30 GHz or greater. As a result, in applications that require simultaneous acquisition and display of multiple wideband signals, scopes that provide more than 30-GHz bandwidth on just two channels often prove to be inadequate because they become, in effect, single-channel instruments.

According to Ken Johnson, LeCroy's marketing director for high-performance scopes, the lifetime in the market of a scope that offers 30-GHz or higher bandwidth on only two channels would be too short to justify its development cost. LeCroy's modular-scope system architecture yields products with greater expected market lifetimes. Customers can upgrade their systems as their needs dictate and can continue using—as parts of their upgraded systems—components they purchased earlier.

Although engineers can upgrade most modern, ultra-high-performance scopes, the upgrades are neither as complete nor as cost-effective as those of modular-scope systems. Johnson says that, over a period of five years or more, LeCroy customers will be able to repeatedly upgrade their modular-scope systems without discarding any of the older components. Thus, in the ultra-high-performance range, even if the sole criterion were economics—and it isn't—the modular architecture would soundly beat a fixed-configuration box.

An LM10Zi-A system comprises a display/control module and one to five acquisition modules. In systems that include several acquisition modules, those modules can be identical or of multiple types. The display is a 15.4-in.-diagonal, 1280×768-pixel, color LCD, which provides significantly greater viewing area than do the 12.1-in. LCDs that are common in high-performance DSOs.

The LM10Zi-A series includes five models of acquisition modules, two of which support DBI. The module sizes come close to the industry-standard multiples of 1.75-in. height and nominal 19-in. width. The display/control module measures approximately 10.5 in. high, and most of the acquisition modules measure approximately 7 in. high. Prices for complete working systems begin at $252,900, which buys a four-channel system that acquires 80G samples/sec on all channels and delivers 25-GHz bandwidth on each. For $411,900, you can buy a system that takes 80G samples/sec on four channels and delivers 36-GHz bandwidth on each or takes 160G samples/sec on two channels and delivers 60-GHz bandwidth on each. You can equip the system with 1.024G points/channel of DBI-mode acquisition memory; 40M points/channel in DBI mode are standard.

The system uses LeCroy's proprietary new SiGe chip set, which the company fabricated with IBM Corp's 8HP manufacturing process. This process yields analog ICs with greater speed and lower noise than do older SiGe processes, which once represented major advances over purely silicon processes.

—by Dan Strassberg

▷**LeCroy Corp**, www.lecroy.com.

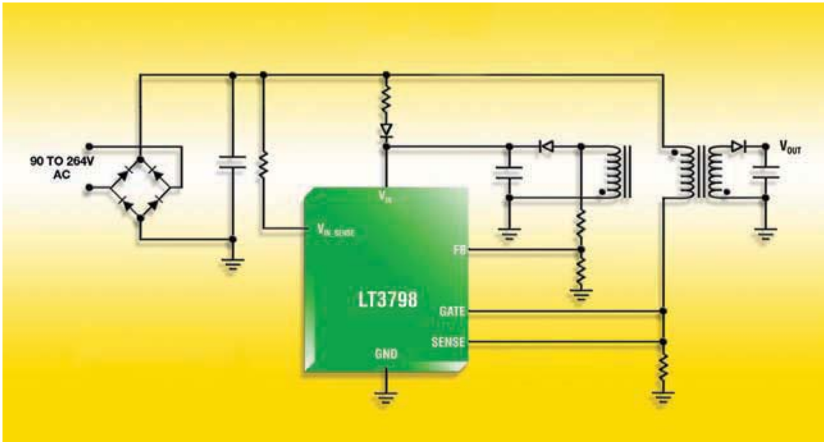
DILBERT By Scott Adams

Offline ac/dc PFC flyback regulator eschews optocoupler; simplifies, improves design

Going from ac-line to dc constant-current/constant-voltage power is a challenge because you must balance the need for sufficient regulation, efficiency, and PFC with the need for low parts count and cost. The LTC3798 from Linear Technology Corp manages the ac/dc transition using a single-stage flyback topology along with isolation. It achieves this task without an optocoupler, or optoisolator, because it senses the output voltage through the primary-side feedback signal. Target applications include high-end LED drivers; 12, 24, and 48V bus converters; and avionic supplies.

Active PFC yields a correction factor greater than 0.97, and the IC typically operates over a 90 to 277V-ac span, supporting output power as high as 100W. Associated external components primarily determine the input- and output-voltage limits, so you can also configure the device for applications requiring input voltages of 400V ac or more. These applications include industrial systems, electric and hybrid vehicles, and medical equipment. The device includes a 1.9A gate driver for controlling an external MOSFET.

Efficiency is typically better than 86%, and output-voltage and -current regulation are typically within ±5%. Using the LTC3798, a designer can develop a circuit that both meets the IEC-61000-3 harmonic-emissions specification and complies with Energy Star requirements of less than 0.5W no-load power.



The LTC3798 flyback regulator from Linear Technology Corp supports ac/dc conversion, along with nonoptically isolated feedback, high power factor, and high-voltage and -current output.

Feedback does not require the use of a transformer; instead, it occurs through an extra winding off the power transformer as part of the CRM (critical-conduction) topology. With nonoptically isolated feedback, the minimum-load requirements are lower than those in optically isolated designs. In a 24V, 1A isolated design, for example, approximately 2 mA goes to the output clamp, and input power is approximately 100 mW.

The LTC3798 has an operating-temperature range of –40 to+125°C and sells for $2.25 (1000). Another version operates at –40 to +150°C. The IC comes in a thermally enhanced, 16-lead MSOP.

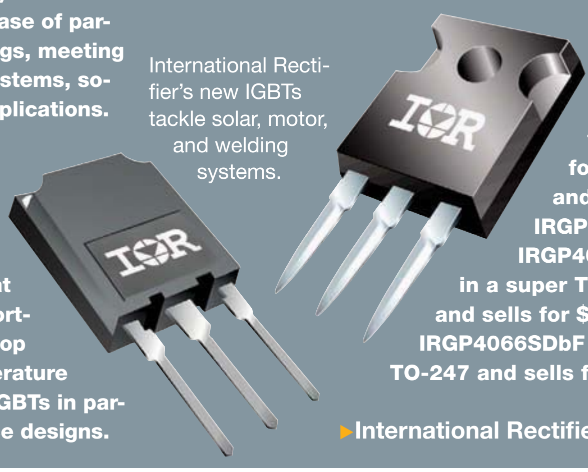
—by Bill Schweber

▷**Linear Technology Corp**, www.linear.com.

IGBTs tackle 600V UPS, solar, motor, and welding applications

01.05.12

Using a trench-insulated process, two new IGBTs (insulated-gate bipolar transistors) from International Rectifier provide fast switching, ease of parallel configuration, and 600V ratings, meeting the needs of higher-power UPS systems, solar power, motors, and welding applications. The IRGP4067DPbF and IRGP4066SDbF feature low conduction and switching losses, along with a low-reverse-recovery-charge diode for soft switching. The IGBTs can switch at 8 to 30 kHz and have a 5-µsec short-circuit rating. Their low voltage drop and a positive-voltage-drop temperature coefficient facilitate using these IGBTs in parallel for high-power, low-resistance designs.



International Rectifier's new IGBTs tackle solar, motor, and welding systems.

Breakdown voltage is 600V, with a charge current of 120A at 100°C for the IRGP4067DPbF and 75A for the IRGP4066SDbF. Both have a 1.9V voltage drop. Thermal resistance is 0.20°C/W for the IRGP4067DPbF and 0.33°C/W for the IRGP4066SDbF. The IRGP4067DPbF comes in a super TO-247 package and sells for $5.58 (10,000); the IRGP4066SDbF comes in a standard TO-247 and sells for $4.80.

—by Bill Schweber

▶**International Rectifier, www.irf.com.**

Microcontrollers sip electrons; target smart-meter, monitoring, and medical apps

A new group of microcontrollers from Silicon Labs decreases power consumption for battery-operated wired and wireless embedded systems.

A new group of microcontrollers from Silicon Labs decreases power consumption for battery-operated wired and wireless embedded systems. The C8051F96x microcontroller and Si102x and Si103x wireless microcontrollers offer approximately 65% more runtime than competing approaches. The wireless version of the basic microcontroller adds the company's less-than-1-GHz EZRadioPro transceiver to the single-chip design, supporting a range of frequencies and formats. Basic operation of the device requires less than 300 nA at 3.6V.

The design minimizes active-mode time using dedicated hardware accelerators for AES (Advanced Encryption Standard), DMA (direct-memory access), CRC (cyclic-redundancy check), SPI, and other functions. Sleep mode uses an ultra-low-power RTC, multiple RTC alarms, and an enhanced LCD driver with an integral charge pump. Active mode uses an on-chip dc/dc buck converter with efficiency of as much as 85% with selective clock gating. A dedicated packet-processing engine speeds RF-message-packet handling by a factor of five and allows longer sleep periods, critical to lower overall energy use.

The devices include hooks that make them compatible with meter installations, such as a direct interface to meter registers, and an analog front end that measures pulses and switch closures. Each device includes a 12-bit, 16-channel ADC; current comparators; and a current reference. Other meter-friendly features support Form A, Form C, and quadrature encoding from the meter transducer, along with back-flow and flutter detection, which are attributes of available meter designs; programmable pullup resistors; dynamic self-calibration; programmable switch-closure debouncing; and wake-up on match or error conditions. Sleep current from a 3V supply is 400 nA with the RTC running and 70 nA with the RTC disabled; wake-up time is just 2 μsec.

The Si102x and 103x provide sensitivity of –121 dBm and output power of 20 dBm, using integrated low-noise and power amplifiers, respectively, yielding a link budget of 141 dB and range as long as 3 km. Operating frequency is 240 to 960 MHz. The ICs include an antenna-diversity algorithm and FIFO, packet-handler, wake-up-timer, and low-battery-detection functions. The devices differ in internal processor functions.

A baseboard and microcontroller or a wireless picoboard is available, and the development system is compatible with the vendor's tools as part of an integrated development environment; a wireless development suite is also available. The development-kit baseboard includes a multiplexed LCD driver, a USB-based debugging adapter, a power supply, a battery, cables, and documentation. Software includes code samples for the various hardware peripherals, such as DMA and management of the dc/dc converter.

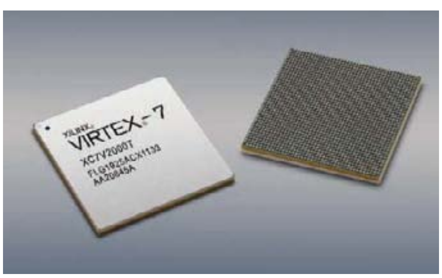
All devices are available for sampling, and full production begins during this quarter. Prices for the C8051F96x begin at $2.41 (10,000), and the Si102x and Si103x sell for $4.39 and $3.27, respectively. Development systems and tools sell for $199 to $299 for the C8051F96x and $829 for the wireless units. The Si102x and Si103x come in 6×8-mm, 85-pin LGA packages, and the C8051F96x is available in three package styles spanning 40 to 80 leads.

—by Bill Schweber

▷**Silicon Laboratories Inc**, www.silabs.com.

Xilinx announces highest-capacity FPGA

Xilinx has announced the first shipments of its Virtex-7 2000T FPGA, currently the highest-capacity programmable-logic device. It contains 6.8 billion transistors and provides users with 2 million logic cells, which is equivalent to 20 million ASIC gates. This high capacity makes the Virtex-7 2000T ideal for system integration, ASIC replacement, and ASIC prototyping and emulation. Xilinx's SSI (stacked-silicon-interconnect) technology makes possible the high integration. The application of 2.5-D IC stacking gives customers twice the capacity of competing devices and leaps ahead of what Moore's Law could otherwise offer in a monolithic 28-nm FPGA.



Xilinx's Virtex-7 2000T FPGA is currently the highest-capacity programmable-logic device.

The Virtex-7 2000T FPGAs have sufficient capacity to replace large ASICs and to achieve overall comparable total costs in a third of the time, creating integrated systems that increase system bandwidth and reduce power by eliminating I/O interconnect, and accelerating the prototyping and emulation of advanced ASIC systems.

Xilinx is now shipping initial engineering samples. Visit www.xilinx.com/virtex7 to see the demonstration of the first Virtex-7 2000T device using more than 70% of its resources at a fraction of the power of an equivalent design in multiple FPGAs. **—by Clive Maxfield**

▷**Xilinx**, www.xilinx.com.

Quad, octal 12- and 14-bit ADCs target communication, medical needs

A quartet of 12- and 14-bit ADCs from Analog Devices offers a variety of channel densities, sampling rates, and packaging options, including a choice of four or eight channels, available nonmagnetic packages for MRI (magnetic-resonance-imaging) designs, and sampling rates. The eight-channel converters feature 40% lower power dissipation than competitive devices, according to the vendor. Target applications include medical, wireless-communications, and industrial designs.

The 14-bit, eight-channel AD9257; 12-bit, eight-channel AD9637; 14-bit, four-channel AD9253; and 12-bit, four-channel AD9633 ADCs feature a serial-LVDS interface; a low-power, reduced-output-swing option; data- and frame-clock outputs; and operation from a single 1.8V power supply. They also offer a 650-MHz, full-power analog bandwidth; a 2V-p-p input-voltage range; serial-port control; and operation over the industrial-temperature range of –40 to +85°C. The SNR ranges from 71.8 dBFS to 75.7 dBFS, depending on the converter.

The four-channel, 12-bit, 80M-sample/sec AD9633 ADC is part of a family offering a variety of sampling speeds and options. The devices target communication and medical needs.

The four-channel units are available in nonmagnetic packages, making the devices ideal for MRI systems. The converters may be placed closer to the signal of interest, which can increase the quality of image resolution and image throughput while reducing the overall component count.

The AD9257 comes in a 64-lead, 9×9-mm LFCSP. The 40M- and 65M-sample/sec units sell for $46 and $71 (1000), respectively. The AD9637 comes in a 64-lead, 9×9-mm LFCSP. The 40M- and 80M-sample/sec units sell for $40 and $56, respectively. The AD9253 comes in a 48-lead, 7×7-mm LFCSP; has sampling rates of 80M, 105M, and 125M samples/sec; and sells for $63, $100, and $117, respectively. The AD9633 comes in a 48-lead, 7×7-mm LFCSP; has sampling rates of 80M, 105M, and 125M samples/sec; and sells for $44, $58, and $69, respectively.

> The 12- and 14-bit, four- or eight-channel ADCs offer a variety of channel densities, sampling rates, and packaging.

—by Bill Schweber

▷**Analog Devices Inc**, www.analog.com.

Resettable low-voltage electronic fuses ease hot-swap design, provide warning

Fusing to prevent overcurrent damage is critical in hot-swap design. Targeting this need, the 5V STEF05 and 12V STEF12 electronic fuses from STMicroelectronics can replace larger conventional fuses or other protection devices. Unlike fuses, however, they neither suddenly cut the power nor require replacement after actuating. The 3×3-mm devices restrict the supply current, thus protecting the connected circuitry, and ultimately turn off the protected equipment if the fault persists.

You can reset them using a signal from the system or by restarting the power supply.

The devices provide a signal when they are intervening, allowing the system to generate a warning. If the fault persists after the reset, the fuse immediately limits the current and turns off again to protect the circuitry.

The 5V STEF05 and 12V STEF12 electronic fuses replace larger conventional fuses or other protection devices.

The devices also integrate circuitry that limits voltage fluctuations applied to the protected load, as well as programmable start-up time through an external capacitor—a necessary function in hot-swap systems. You use an external resistor to set the current limit. The STEF05 and STEF12 come in 10-lead, 3×3-mm DFN packages, and prices start at 75 cents (1000).

—by Bill Schweber

▷**STMicroelectronics**, www.st.com.

BY HOWARD JOHNSON, PhD

Quadrature-connector layout

Some ideas are just too good to keep to yourself. **Figure 1** illustrates the blueprint for a differential connector that radically reduces crosstalk between nearest-neighbor pairs. This cross-sectional view of a nine-pair connector shows the arrangement of 18 flat pins as they pass through the body of a connector. Each pair of pins comprises a broadside configuration, meaning that the broad sides of the two pins face each other.

Many differential connectors use broadside coupling. The Molex I-Trac, for example, uses broadside-coupled differential pairs with no additional solid reference layers. If a user requires additional grounds, the grounds are assigned to ordinary data-pin locations.

Other differential connectors use edge-coupled pins. For example, the Ernie ERmet ZD uses edge-coupled pairs with solid-plane layers between rows of pins. The FCI Airmax VS uses edge-coupled pairs with no solid reference layers.

In the Molex, Ernie, and FCI designs, the pairs appear in a regular array, with all of the pairs arranged in the same orientation. The unique aspect of the connector in **Figure 1** is not the use of broadside coupling but the alternating 90° rotation of every other pair. The orientation of Pair H, for example, is rotated 90° with respect to the orientation of Pair G. In this quad-connector layout, each pair is rotated into a position that stands in quadrature to its nearest neighbors.

The quadrature alignment dramatically reduces crosstalk. To see why, examine the curved lines in **Figure 1**. They represent magnetic lines of force that the central pair creates when they are operated in a differential mode. In a cross-sectional diagram such as this one, the crosstalk a victim pair receives varies in proportion to the number of magnetic lines of force that pass between the two elements of that victim pair, crossing perpendicular to the axis connecting the two elements. A line passing parallel to the axis connecting the two elements causes no crosstalk (**Reference 1**).

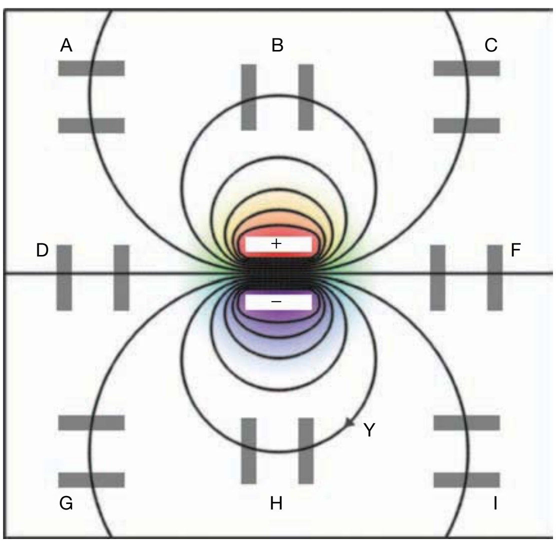


Figure 1 This differential-quadrature-connector layout suppresses nearest-neighbor crosstalk.

Consider victim Pair H, which uses a side-by-side layout. Field Line Y passes straight from one element to the other, parallel to their axes, without passing between the two of them. That orientation eliminates unwanted crosstalk from Field Line Y. If Pair H had used an over-and-under orientation, as the central pair does, Line Y would have penetrated the space between the elements of H in a perpendicular direction, causing crosstalk. That arrangement is the usual one in a connector and one of the main drawbacks of a uniformly oriented pin array.

The benefits of exact quadrature layout also accrue to pairs B, D, and F, which each pick up zero differential crosstalk from the central pair. The arrangement in **Figure 1** suppresses crosstalk from the central pair to each of its next four nearest neighbors, A, C, G, and I, as an ordinary connector would.

A practical quad connector must solve the problems of how to twist the pins to obtain the correct alignment and how to maintain a consistent quadrature alignment moving all the way down through the PCB attachment into the underlying PCB.

If these problems prove tractable, a practical low-crosstalk connector would permit the design of serial links with larger link-loss budgets than is now possible, enabling the use of multilevel signaling, which greatly boosts the effective digital bandwidth. EDN

REFERENCE

1 "Quadrature-via layout," *EDN*, Dec 1, 2011, pg 20, http://bit.ly/viAVnt.

Howard Johnson, PhD, of Signal Consulting, frequently conducts technical workshops for digital engineers at Oxford University and other sites worldwide. Visit his Web site at www.sigcon.com, or e-mail him at howie03@sigcon.com.

BY PALLAB CHATTERJEE

Storage relies on DRAM

As capacity and performance increase for computer storage in both enterprise and network-endpoint units, systems are increasingly reliant on DRAM in these products (**Figure 1**). The DRAM use has helped meet the performance requirements, observe the physical limits, and hold the power factor. Hard disks and most rotating media, such as optical disk drives, have a mechanical speed limitation that keeps their data coming off the read head at rates on the order of hundreds of megabits per second. However, most of the interfaces in use today, such as SATA, USB, and Thunderbolt, are all multiple-gigabit-per-second interfaces.

Typical state-of-the-art disk drives operate at 7200 rpm and have access times of less than 10 msec. To achieve interface rates between these access times and the 3- to 6-Gbps SATA, system engineers have been adding more cache memory to the drives themselves. The standard for years was 16 Mbytes, and now most of the systems feature 32 or 64 Mbytes. The increase in memory allows the use of inexpensive controllers that can be directly integrated into the chip set and the CPU. These integrated controllers generally support either a SATA format or a PCIe interface. For enterprise systems, stand-alone controllers still support drives using SAS (serial-attached SCSI) or SOP (SCSI over PCI), which is gaining popularity as an interface.

These systems are using low-power memories. Designers of higher-capacity drive memories are also seeking power reduction and are moving from memories requiring 2.5V to those requiring 1.8V. This shift will help to reduce power but retain the same access times. The use of DRAM is a key component for performing ECC (error-correction code) on the data both entering and exiting the system bus. Unlike solid-state disks, which have a lower bit-error rate, rotating media—even those in consumer-targeted drives—have a data-integrity requirement on the order of one part in 10^{14}.

Self-encrypted drives are also fueling the need for increased DRAM in hard drives. These self-encrypted devices need a working area to encrypt and decrypt the message strings. The data strings can be as long as 2048 bits, and the processing of these strings can take many megabytes of DRAM. Self-encrypting drives typically have 64 Mbytes or more of cache memory to facilitate this operation and to maintain the multiple-gigabit-per-second throughput.

Solid-state disks and hybrid drives also heavily rely on DRAM. Although these drives are faster by a factor of 100 than rotating media, their read- and write-cycle times are still in microseconds. The data connections still need nanosecond- and microsecond-level data access, so designers use DRAM to manage these times. The discrepancy between nanosecond and microsecond performance is much less than that of the multiple-millisecond access of the rotating media. The DRAM for solid-state and hybrid drives is smaller, so designers can typically integrate it into the controllers.

The Thunderbolt interface operates at 10 Gbps—more than 1 billion times faster than the data rate of rotating media and 1 million times faster than solid-state drives. Its storage is thus primarily DRAM in several-gigabyte blocks. Professional systems will be implemented with ECC DRAM and support dual read and write paths, prior to the actual storage media. EDN

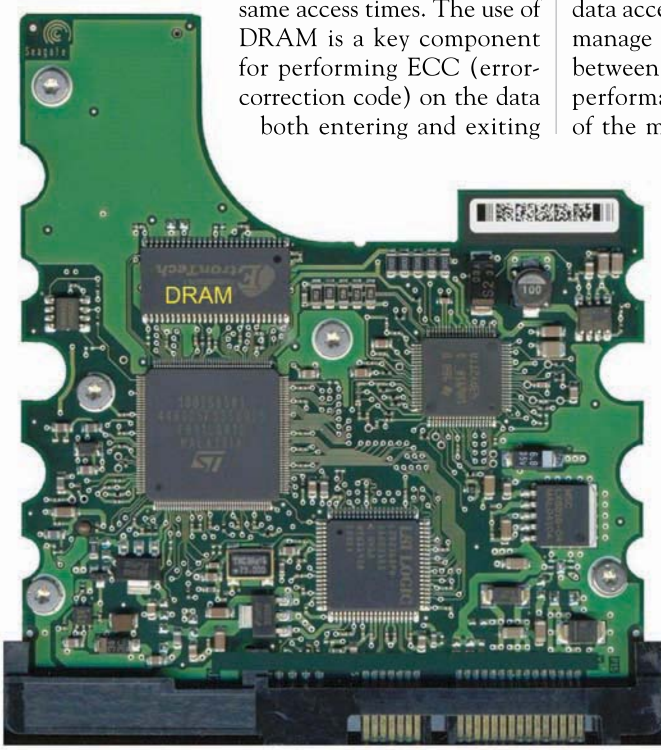
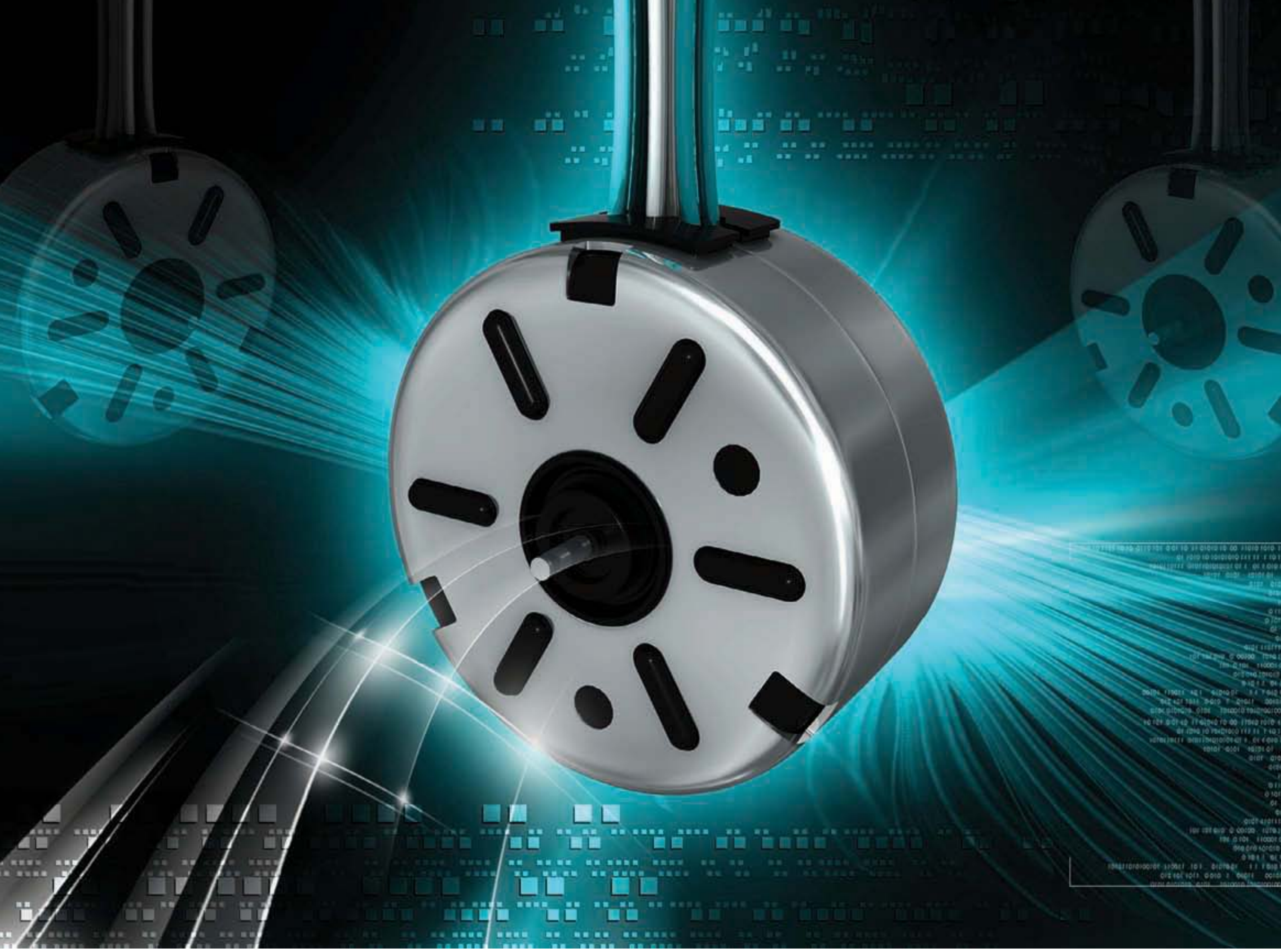


Figure 1 Systems are increasingly reliant on DRAM in products such as hard-disk and solid-state drives (courtesy Seagate).

Pallab Chatterjee has been an independent design consultant since 1985.



BACK-EMF METHOD DETECTS STEPPER-MOTOR STALL

DAVID SWANSON AND RADEK STEJSKAL • STMICROELECTRONICS

AN INNOVATIVE TECHNIQUE TAKES ADVANTAGE OF CONSTANT MOTOR PARAMETERS AND OVERCOMES THE LIMITATIONS OF TRADITIONAL STALL-DETECTION METHODS OF CURRENT AND DUTY-CYCLE SENSING.

Stepper motors find use in many automotive applications, including headlight leveling; adaptive headlamps, in which the headlamps turn right or left with the steering wheel; EGR (exhaust-gas-recirculation) valves; and adjustable mirrors. Nonautomotive apps for the method include any stepper motor with a current of approximately 1A.

Stepper motors seem to be fairly straightforward machines. They are essentially slaves to controllers, which perform commutation when they want to without regard to the stepper motor. The controller requires no feedback to help with appropriate times to commutate.

IMAGE: SHUTTERSTOCK

In comparison, a brush-type motor commutates when it wants to and doesn't require the controller to perform any commutation. The BLDC (brushless-dc) motor, a close relative of the stepper motor, tells the controller when it wants to commutate.

Because a stepper motor acts as a slave, you must drive it well beyond what is necessary to ensure that it moves and stops when told. The stepper-motor controller needs no feedback.

Even in a stepper motor, however, feedback can be desirable. For instance, it would be nice to know whether the motor has stalled. You can look for feedback on the state of the motor by polling a third party, such as a position sensor, or you can look to the motor itself for rotational information. You can perform these tasks using motor-current monitoring as a reflection of back EMF, or BEMF (back electromotive force). Alternatively, you can look directly at BEMF.

External components to monitor motor position can add cost to the system. You can, however, get what you need without adding components or cost.

L9942 STEPPER MOTOR

The integrated L9942 stepper-motor driver for bipolar stepper motors operates in automotive-headlamp leveling. The device offers a programmable current-profile look-up table to allow for flexible adaptation of the stepper-motor characteristics and intended operating conditions. In other words, it can do full stepping, half-stepping, and microstepping. The L9942's microstepping mode provides for 32 programmable current-regulated steps over 360°, translating to eight levels of current per quadrant (**Figure 1**).

PWM control regulates each step current. An oscillator fixes the pulse-width modulator's on-time, and the measured current fixes its off-time. The high-side switches provide a current-mirror feedback, which the L9942 compares with a preset, programmable current value through a look-up table. When the current in the phase matches the value in the look-up table, the phase turns off until the PWM's next on-time. As a result, the L9942 approximates a current sine wave in 32 steps through PWM control of the outputs (**Figure 2**).

AT A GLANCE

- Automotive applications for stepper motors may include headlight leveling; adaptive headlamps, in which headlamps turn right or left with the steering wheel; EGR (exhaust-gas-recirculation) valves; and adjustable mirrors.
- Nonautomotive uses for stepper motors are those in which the current is approximately 1A.
- The BEMF (back-electromotive-force) technique takes advantage of constant motor parameters and overcomes the limitations of traditional stall-detection methods of current and duty-cycle sensing that can vary with motor resistance, battery voltage, and temperature.

STALL-DETECTION METHODS

During a stall, the motor current rises quickly because the BEMF is absent. The lack of BEMF increases the potential current in a winding at a given voltage, according to Ohm's Law, and it increases the rate of change of the current in the windings because the rate of change of current in an inductor is proportional to the voltage across the inductor. With little or no BEMF in a motor winding, the current rises quickly (**Figure 3**).

When microstepping, however, the system regulates the motor-phase current by turning off the phase when it reaches the preprogrammed current threshold. As a result, the motor current does not spike when the motor stalls. Instead, the duty cycle decreases to a fairly small value because the current-control algorithm compensates for the loss of BEMF. You detect BEMF loss by observing an abnormally low duty cycle for a given commanded current. The L9942 measures this duty cycle and reports the information back to the host microcontroller through SPI.

The difficulty with this method is that many parameters can move around in the normal operating space of a stepper motor. Temperature, battery voltage, and loading or torque can have a dramatic effect on the current regulation's duty cycle. The operating point at one end of the normal spectrum can look like a stalled motor at the other end. Overlapping parameters make it difficult at best to safely discern a stalled rotor. As a result, it is more difficult than measuring a current or looking at a regulated duty cycle. To minimize the effects of motor resistance, battery voltage, and temperature, the stall-detection algorithm can look directly at BEMF.

BEMF SENSING

Overdriving a stepper-motor phase causes the BEMF to shift by as much as 90°. As a result, in an unloaded stepper motor, the BEMF is highest in a phase when the current is the lowest in that phase (**Figure 4**). You can take full advantage of this phenomenon when sensing BEMF. When the phase current is moving from one polarity to

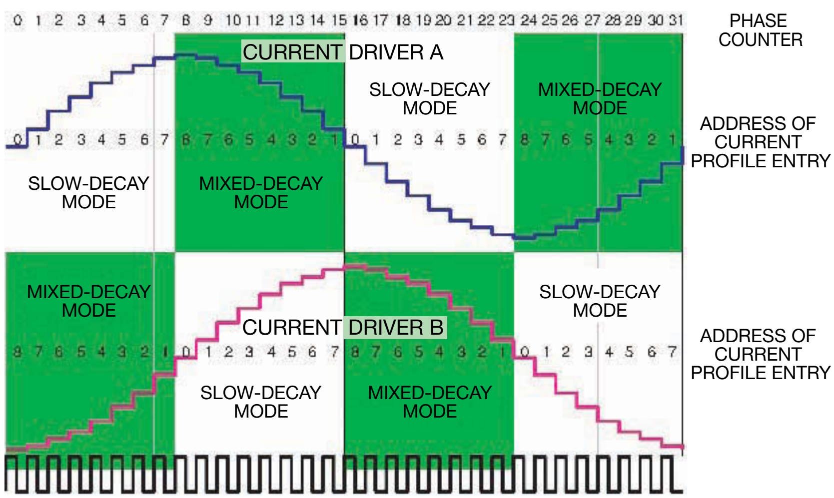


Figure 1 The L9942's microstepping mode provides for 32 programmable current-regulated steps over 360°, translating to eight levels of current per quadrant.

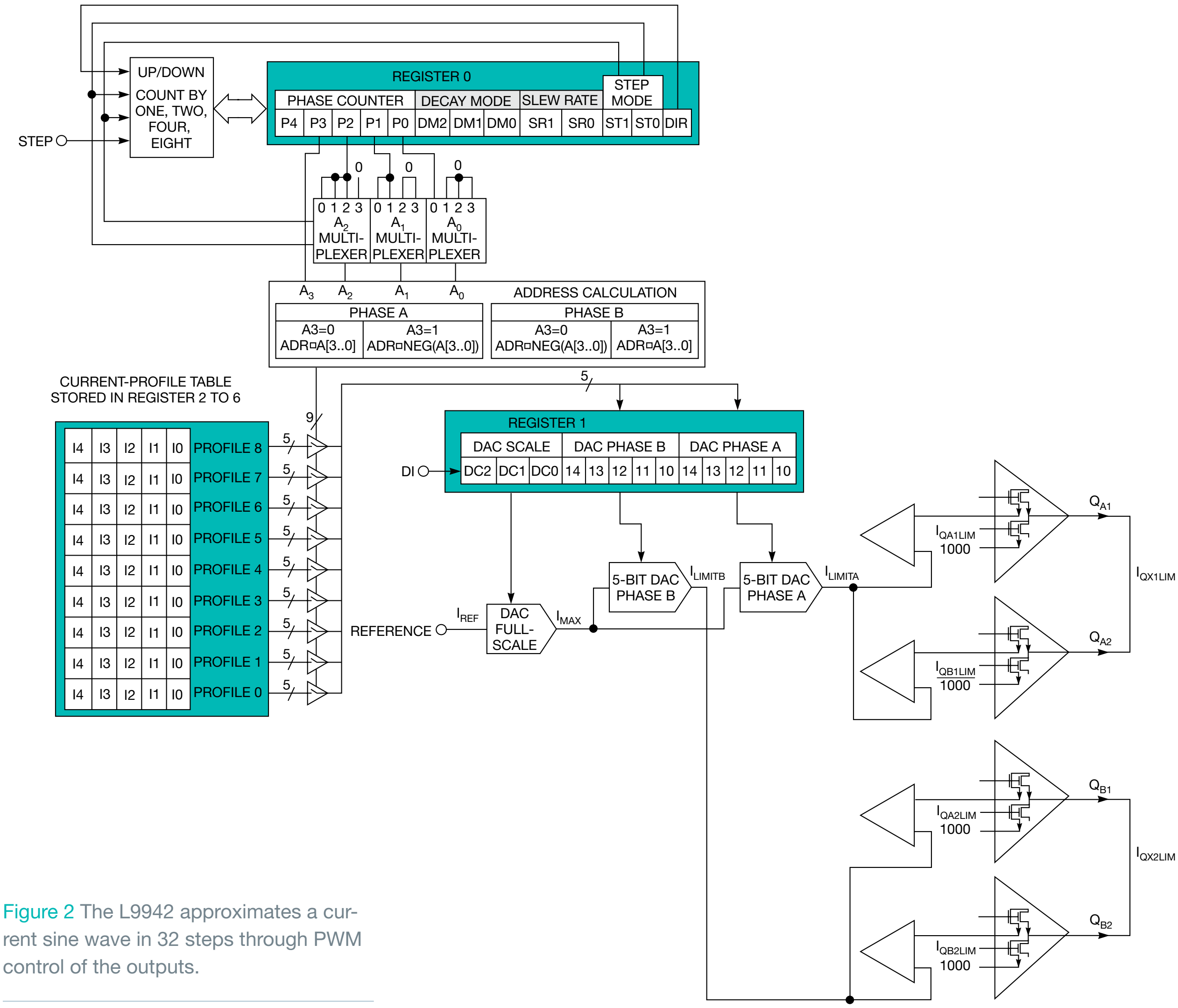


Figure 2 The L9942 approximates a current sine wave in 32 steps through PWM control of the outputs.

the other, the current passes through 0A, meaning that no major issues occur with the inductive flyback when you turn off the phase to look for BEMF (**Figure 5**).

The resulting waveforms look as you would expect. In an unloaded motor, in which the phase current is at or near 0A, the BEMF for that phase is the strongest (**Figure 6**). You must, however, understand the effects of motor loading on the phasing, or phase shifting, of the BEMF. Because this algorithm looks for BEMF only when the phase is not being driven, you have a short window during which to "look." As the motor loads, the BEMF shifts so that it aligns better with the driving voltage and current for that phase. Motor loading adds some variation to the BEMF detection. A fully loaded motor just on the edge of stalling looks the same as a fully stalled motor. Fortunately, a stepper motor is not intended to be driven with that much load.

UNIVERSAL MOTOR CONCEPTS

BEMF is directly proportional to angular velocity, or armature speed, and motor torque is directly proportional to motor current. The following **equation** clearly illustrates the relationship between angular velocity and BEMF: $BEMF=-N\times B\times A\times\omega\times\sin(\omega t)$, where N is the number of coil turns, B represents the magnetic field, A is the area that the motor's magnetic field encompasses, ω is the angular velocity, and t is time. Notice that N, B, and A are all constants specific to the motor construction. They never change unless some dramatic entropy is going on. At that point, BEMF detection is the least of your concerns. Aside from the sinusoidal nature of the signal, BEMF is directly proportional to motor speed and nothing else.

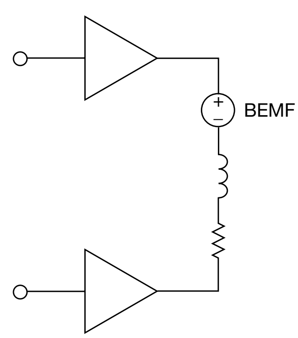


Figure 3 With little or no BEMF in a motor winding, the current rises quickly.

The following **equation** clearly describes the relationship between motor torque and motor current: $T=[(PN)/2\pi)]\varphi I$, where T is torque, N is the number of coil turns, P is the number of poles, φ is the flux, and I is the current. Note again that current and torque are directly proportional to each other. Other factors, including voltage and the temperature's dependence on the resistivity of copper, can increase or decrease the motor current, which in turn affects the total available torque. However, they do not change the torque-to-current relationship.

A stepper motor is typically a fixed-current system—that is, the controller feeds a fixed set of currents into two phases at a rotational velocity that the rotor directly reflects. A fixed current into a motor produces a fixed torque, and, thanks to the automatic phase shifting of the BEMF with respect to drive current, a stepper motor can have

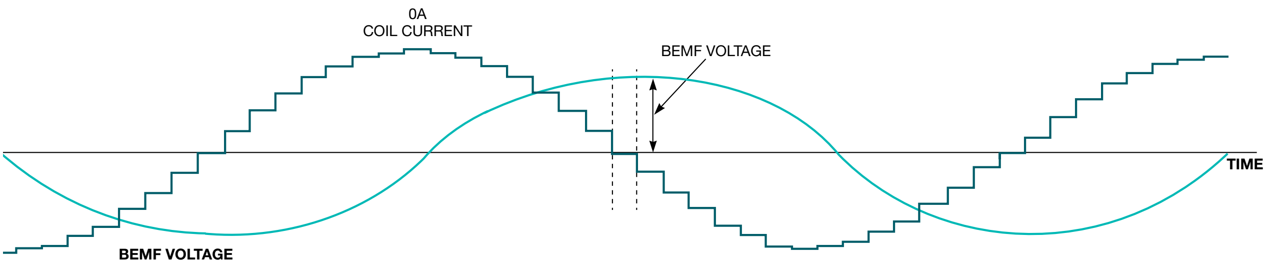


Figure 4 In an unloaded stepper motor, the BEMF is highest in a phase when the current is the lowest in that phase.

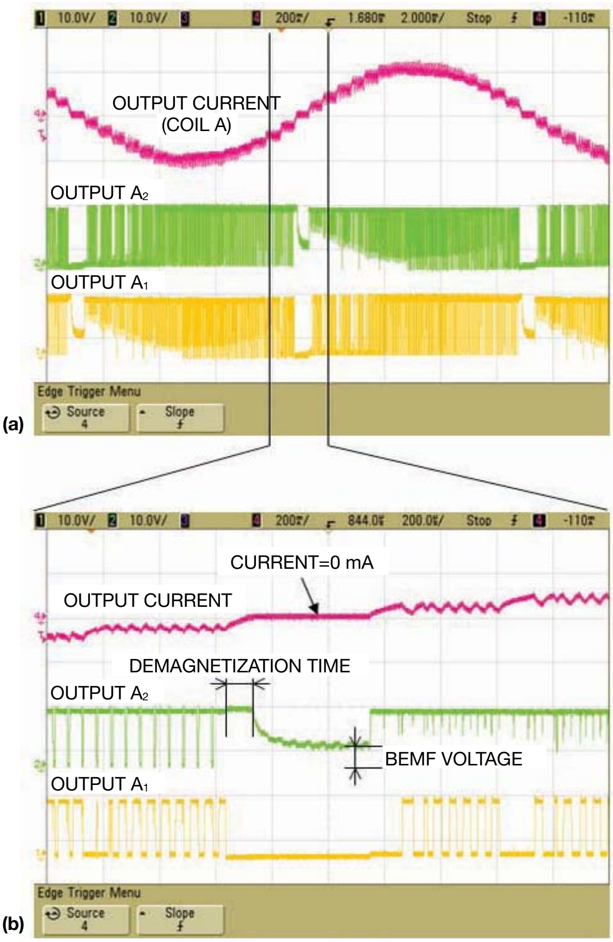


Figure 5 When the phase current is moving from one polarity to the other, the current passes through 0A (a), meaning that no major issues occur with the inductive flyback when you turn off the phase to look for BEMF (b).

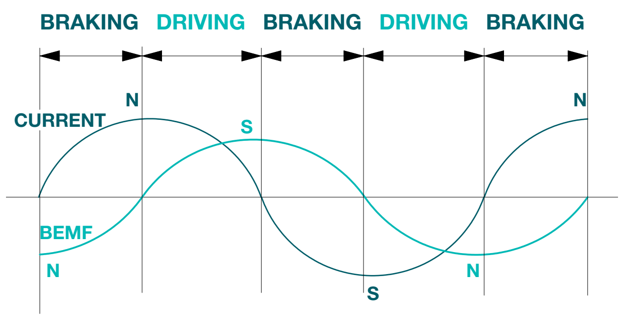


Figure 6 In an unloaded motor, in which the phase current is at or near 0A, the BEMF for that phase is the strongest.

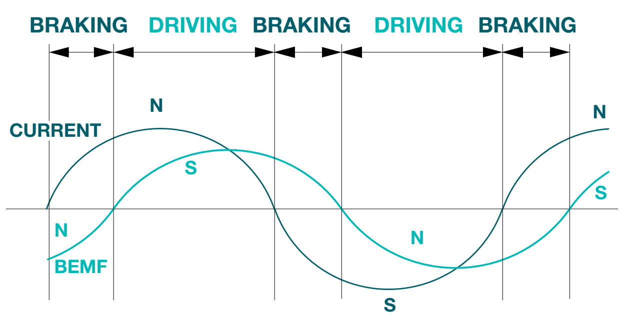


Figure 7 In a partially loaded stepper motor, the BEMF has shifted to increase the percentage of driving torque over the braking torque.

a fixed current and rotate at a fixed speed for a range of loads or torques.

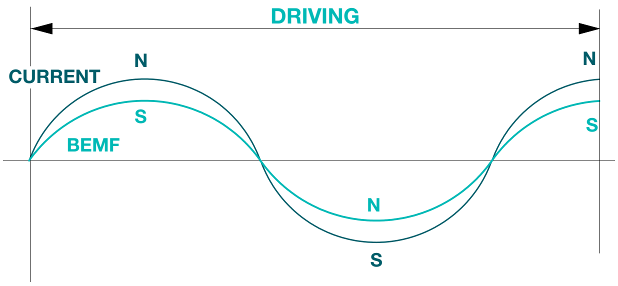


Figure 8 The BEMF shift continues as external loading increases until the loading exceeds the potential torque capability.

The phase current generates the torque using the preceding **equations**. The load determines in which direction to apply that torque. In a lightly loaded stepper motor, a small portion of the torque drives the load, and the remaining torque slows down the motor. To remain below the commanded rotational speed, the current first drives the motor to go faster and then brakes it to go slower. The overall torque exiting the output shaft is zero for an unloaded motor.

BEMF also is a representation of rotor position, as the moving magnets in the rotor induce BEMF in the stator. The rotor's magnetic field is fixed to the rotor and rotates with it. The stator field relates to the current in the stator. A positive current in the stator creates a positive field, and vice versa.

With magnetics, as with some people, opposites attract. When the polarity in the stator is the opposite of the rotor, attraction and, thus, acceleration occur. When the polarity

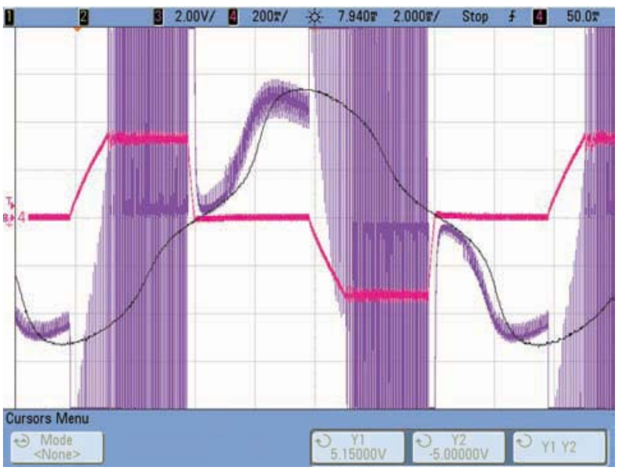


Figure 9 In the motor's full-step mode, the red curve represents the current, and the purple curve represents the voltage on the phase. The thin black curve represents a feeble attempt at estimating the BEMF.

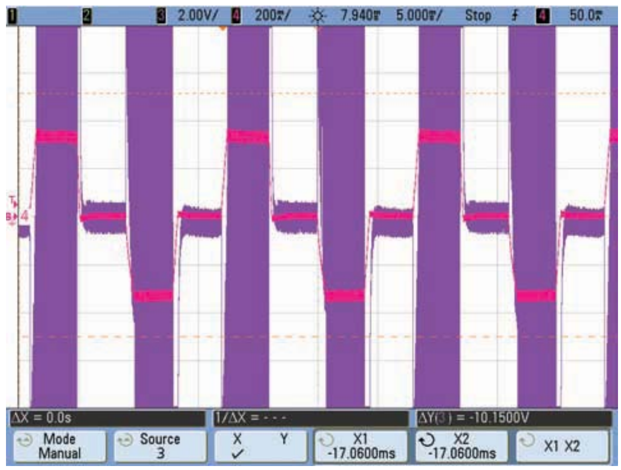


Figure 11 Systems that use stepper motors severely overdrive their motors to ensure that they never, under all normal operating conditions, approach stall. Comparing these waveforms with what appears during stalling shows a dramatic difference, with virtually no BEMF during nondriven intervals.

Figure 10 The loading for a loaded motor is more in line with the current it is receiving.

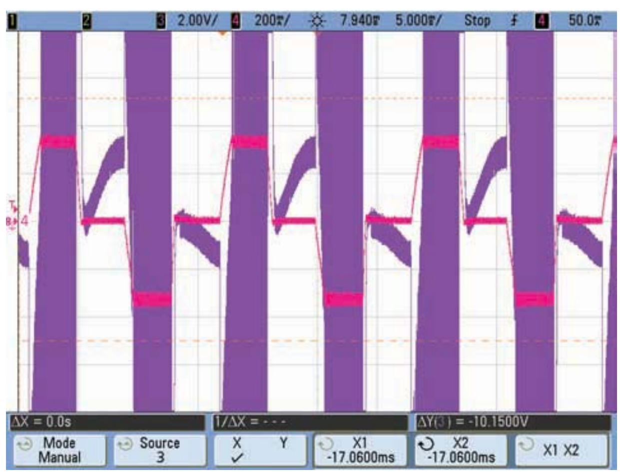


Figure 12 A stalled but vibrating rotor shows an issue with BEMF detection.

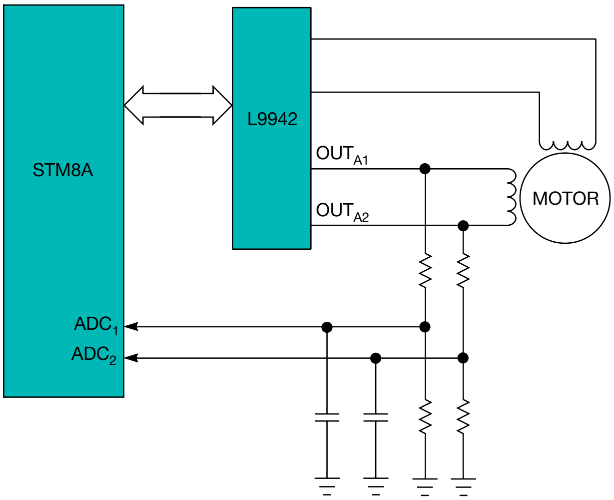


Figure 13 To get some idea what the BEMF looks like on average for a given motor, a simple system checks BEMF synchronously with stepper-motor phasing.

is the same in both the rotor and the stator, braking occurs. In an unloaded motor, you get an almost-perfect distribution of acceleration and braking. As the stepper motor loads, the BEMF shifts to convert more of the torque to forward motion and less to braking.

In a partially loaded stepper motor, the BEMF shifts to increase the percentage of driving torque over the braking torque (**Figure 7**). This shift continues as external loading increases until the loading exceeds the potential torque capability (**Figure 8**).

In a fully loaded stepper motor, the moment that the torque demand causes the BEMF to shift any further, the output torque decreases, and the motor stops rotating. To more easily see the effects of torque on BEMF, look at a stepper motor in full-step mode (**Figure 9**). The red curve represents the current, and the purple curve represents the voltage on the phase. The thin black curve represents a feeble attempt at estimating the BEMF.

In an unloaded motor, the BEMF leads the phase current. The **figure** shows a skewed BEMF peak and a prolonged near-zero period, which represents the torque first speeding up and then slowing down the rotor. Just spinning the motor would provide a symmetrical BEMF waveform.

The loading for a loaded motor is more in line with the current it is receiving (**Figure 10**). The BEMF is more sym-

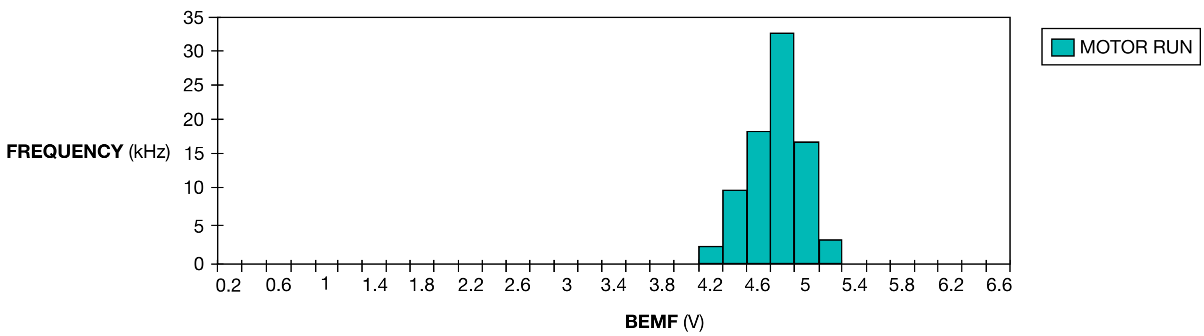


Figure 14 The ADC takes its sample at the end of the zero-current step, ensuring the most consistent BEMF readings. The mean voltage is 4.7278V; the standard deviation is 0.2007V; and the minimum and maximum voltages are 3.6 and 6.6V, respectively.

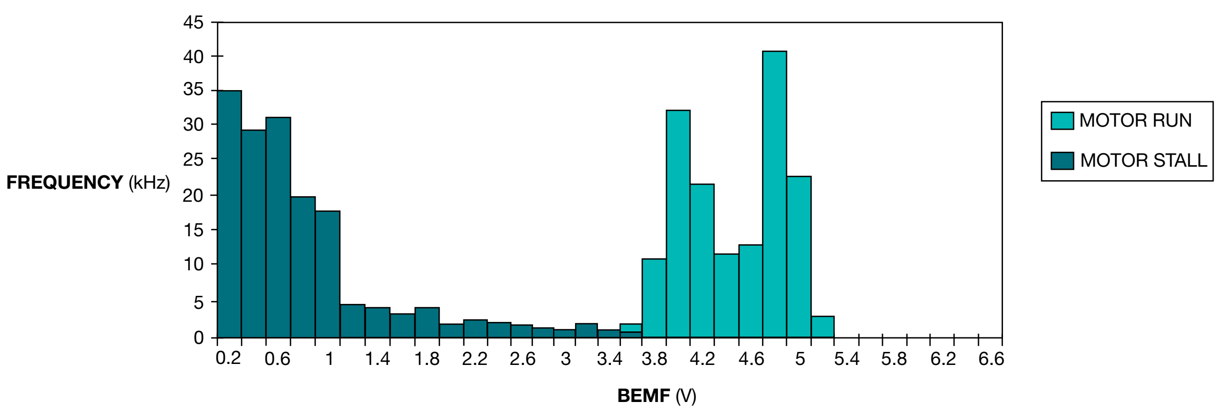


Figure 15 Compare the BEMF results with a stalled rotor and a running rotor.

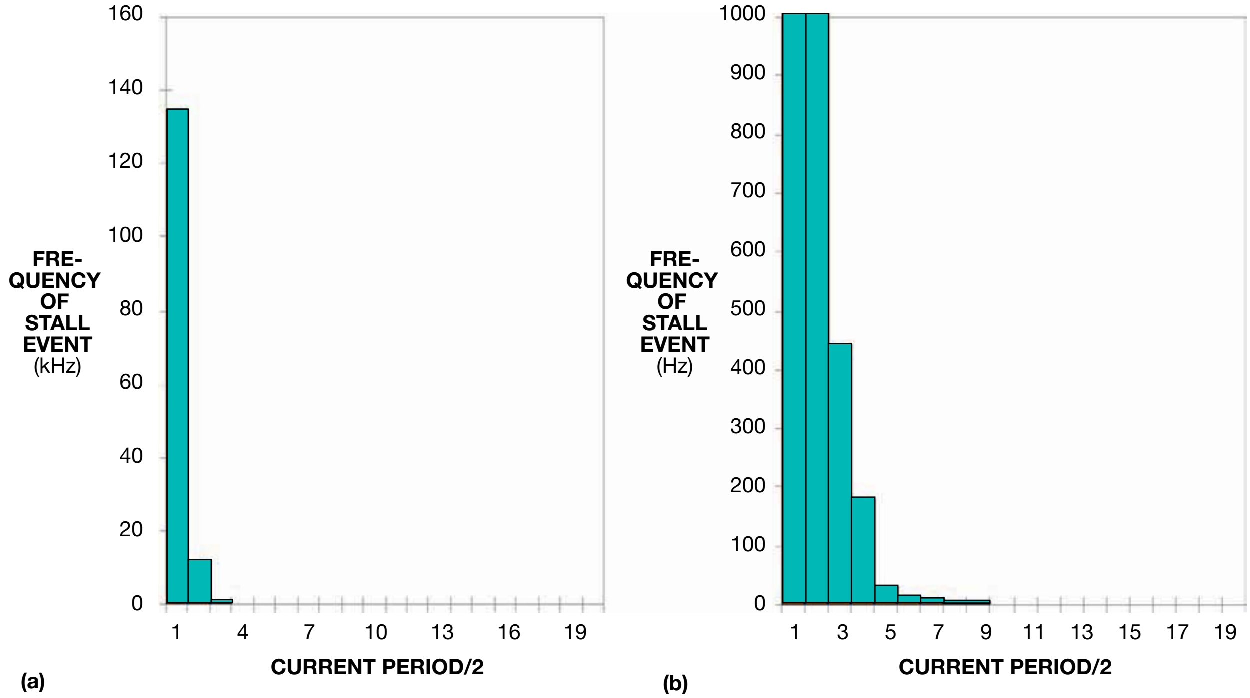


Figure 16 In some instances, the stalled rotor's BEMF shows some variance and overlaps with the running motor's BEMF readings (a). This result is due to motor vibration, which causes BEMF to be more than 0V during the ADC sample (b).

metrical with the driving currents. The zero-crossing point is in the middle, or between the two driving-current regions. If you were to further load this motor, it would stall.

Systems that use stepper motors severely overdrive their motors to ensure that they never, under all normal operating conditions, approach stall. Comparing these waveforms with what appears during stalling shows a dramatic difference, with virtually no BEMF during nondriven intervals (**Figure 11**). Typically, a stalled rotor vibrates as it tries to move; however, any rotational movement translates to BEMF. A stalled but vibrating rotor shows an issue with BEMF detection (**Figure 12**).

These waveforms overlap somewhat with the previous ones. This **figure** shows the behavior of a full-step-mode-driven motor, which differs from a microstep-mode-driven motor. When you are using microstep mode, you are looking only during that short moment when the current is 0A. You can see only a small portion at a time. It may seem limiting, but it is enough. To get some idea of what the BEMF looks like on average for a given motor, a simple system checks BEMF synchronously with stepper-motor phasing (**Figure 13**). With a microprocessor's analog-to-digital sampling, you can quickly obtain several thousand BEMF readings and generate a histogram of the values.

HISTOGRAMS AND LIMITS

The L9942 stepper motor uses an 8-bit STM8A microcontroller, which can synchronously sample the BEMF in step with the L9948. The step-clock frequency for the L9942 is 2 kHz, and the peak current in microstepping mode is 400 mA. The ADC takes its sample at the end of the zero-current step, ensuring the most consistent BEMF readings (**Figure 14**). Compare the BEMF results with those for a stalled rotor and a running rotor (**Figure 15**). In some instances, the stalled rotor's BEMF shows some variance and overlaps with the running motor's BEMF readings. This result is due to motor vibration, which causes BEMF to be more than 0V during the ADC sample (**Figure 16**). Statistically, this overlap is minimal; BEMF is usually lower than this **figure** shows. By setting the BEMF threshold at approximately 2V, a reliable detection can take place because most BEMF measurements are well below that level. If you look at the time it takes to effectively detect stalling for this motor, you find that you can detect the stall within one mechanical revolution of the motor. A current period is the time it takes to make one full 360° electrical rotation. This example steps 32 times at 2 kHz for one full period, translating to 16 msec per period. Within 10 half-periods, or 80 msec, the system detects stall 100% of the time.

These cases compare an unloaded motor with a stalled motor. The differences between these two states are dramatic and easily detectable. From this analysis, you can see that a loaded motor causes the detected BEMF thresholds to drop as the BEMF shifts to align with current. You must take this drop into account when considering an acceptable stalling threshold. Every application has a maximum expected torque requirement, which must be taken into account when determining the BEMF stall threshold. A loose or spongy transmission or a soft stall, in which the rotor can bounce, may also affect these limitations, which are even more difficult to overcome using the current and duty-cycle method. Because the BEMF sensing takes place outside the IC, you can to some extent overcome this limitation with a statistical method discerning the stall threshold.

SYSTEMS THAT USE STEPPER MOTORS SEVERELY OVERDRIVE THEIR MOTORS TO ENSURE THAT THEY NEVER, UNDER NORMAL CONDITIONS, APPROACH STALL.

The BEMF method for detecting stall while using the L9942 can be reliable and cost-effective. This method takes advantage of motor parameters that change little with time or temperature. As a result, this method overcomes many of the limitations of the more traditional stall-detection method of current and duty-cycle sensing. At least one automotive headlamp application uses this algorithm.EDN

ACKNOWLEDGMENT

This article originally appeared in two parts on EDN's sister site, Automotive Designline. *Read part one at http://bit.ly/tVHk2V and part two at http://bit.ly/uTJ1Tm.*

AUTHORS' BIOGRAPHIES

David Swanson is principal engineer in STMicroelectronics' automotive business unit. He has been with the company since 1987. Before joining ST, Swanson worked for the Delco products division of GM. He graduated with a bachelor's degree in electrical engineering from North Carolina State University—Raleigh and holds many patents in several areas of automotive electronics.

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THE PROTOTYPE COMES OF AGE

A RADICAL CHANGE IS ABOUT TO HAPPEN IN THE TYPICAL DEVELOPMENT OF AN ELECTRONIC SYSTEM. THE HARDWARE-DEVELOPMENT FLOW WILL NO LONGER BE THE CENTER AROUND WHICH EVERYTHING ELSE REVOLVES.

BY BRIAN BAILEY • CONTRIBUTING TECHNICAL EDITOR

Over the past few years, interest in prototyping electronic designs has grown. The rising size and complexity of systems and the limitations of using a single-purpose model—the hardware-design model—have fueled this growth. Engineers have traditionally modeled the hardware-design model at the RTL (register-transfer level) and then performed a number of refinement steps until that model becomes the implementation model. This single-purpose model has in the past found use only in hardware design, although engineers are now considering its use for other purposes. The EDA industry has developed tools, such as equivalence checkers, to ensure that the functionality of this evolving model stays consistent during these transformations. In an ideal world, all modifications would apply to the single model at the start of the chain, and changes would propagate throughout the chain. In the real world, however, engineers make changes to the subsequently derived models, potentially leading to departures between the original high-level model and the final implementation. This area has always been regarded as a risk in the development cycle, and that risk increases as additional independent models are generated throughout the flow.

IMAGE: SHUTTERSTOCK


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Debugging

The single hardware-design model can no longer provide all of the functions users demand. The rapid increase in software content means that its development, debugging, and integration cannot be left until first silicon comes back from the fab. The RTL model is too slow for the effective performance of these tasks because it contains implementation details that software execution does not require. Engineers have used emulation to speed the RTL model, but this approach is still too slow, and it is often too expensive for manufacturers to make available to software-development teams. Engineers need faster and cheaper prototypes that are available much earlier in the design flow.

TIME FOR CHANGE

Among the changes now taking place in this area is the migration to higher levels of abstraction for hardware design. Driving this change is a desire for increased productivity in the hardware that provides unique value in a product. The ability to derive several implementations from a single high-level description is also desirable. Once you develop this block at an abstract level and verify it, you can then use it to generate several microarchitectures or target implementation technologies, each with characteristics such as low power or small size. High-level synthesis is helping in this area. As a by-product of high-level synthesis, verification teams have discovered that their process can become more efficient when they use abstract models. As systems become more concurrent, it is no longer possible to analyze the throughput, latency, or other aspects of a system architecture using static methods, so the role of verification is also increasing to include system-level concepts.

Another change affecting hardware- and software-development teams is that more functionality is being provided by reuse—either internal or acquired from third parties. The size, sophistication, and number of these blocks are increasing, and the verification approach for these blocks differs from the approaches you would use for new blocks. Many hardware blocks now come with sophisticated software stacks, and they also must be integrated into the software flow. These changes have led many development teams to the conclusion that they must develop additional models to enable aspects of a system's design or verification to be performed that are not on the hardware-development path. This new approach in turn signals a radical change in the make-up of a development team. Hardware development is no longer the central hub around which everything else revolves. Instead, the system becomes the focus, and hardware development becomes one of the contributors. The prototype becomes the way in which contributors share information.

AT A GLANCE

- Hardware and software developers, architects, and verification teams all need system models.
- Using the hardware-implementation model for multiple purposes may be unfeasible because it requires designers to make too many compromises.
- Prototypes can exist before, during, or after the development of the hardware-implementation model at the virtual, the rapid prototyping and emulation, and the silicon levels, respectively.
- Successful deployment of a prototype must consider the costs, usage scenarios, team skills, and many other factors.

ROLES OF A PROTOTYPE

The first step in choosing a prototype is to understand the needs and expectations associated with the prototype. Who will create the prototype? When will it be created? For what purpose is it needed? You must fully understand the costs, responsibilities, maintenance, verification, and values of the prototype; otherwise, it will not receive the necessary time and attention. Teams who see a prototype as an unnecessary distraction are setting themselves up for failure, and in many cases this is because the developer of the model and the user of the model will be in different groups—one bearing the cost and the other receiving the value. This situation requires management to take a systems approach to budgeting and staffing rather than viewing each discipline separately.

You can consider prototypes before, during, and after the RTL phase of the hardware implementation. Virtual prototypes are those prototypes that you create before RTL; rapid prototypes are those created during RTL development; and physical, or silicon, prototypes are those systems that emerge after the availability of first working silicon (**Figure 1**).

The increased use of IP (intellectual property), the need for additional productivity, increasing verification complexity, and the desire for microarchitectural exploration are some of the changes affecting the hardware developers. Abstraction is important for productivity and exploration, but cycle accuracy is still important for detailed verification. Meanwhile, soft-

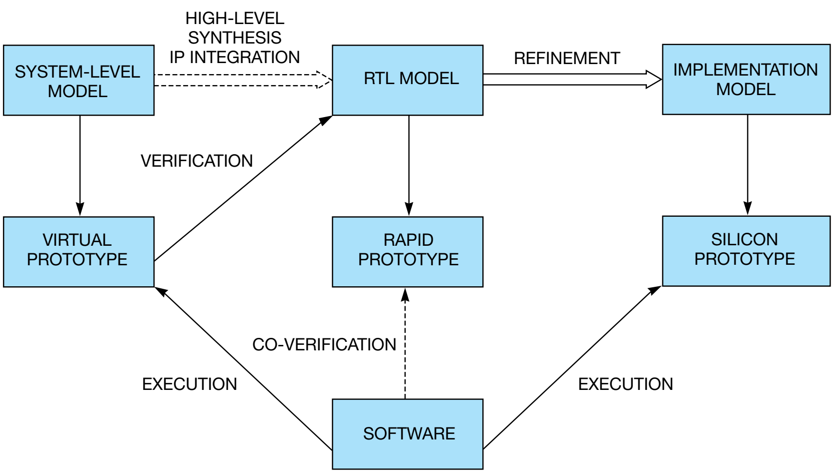


Figure 1 Virtual prototypes are those prototypes that you create before RTL; rapid prototypes are those created during RTL development; and physical, or silicon, prototypes are those systems that emerge after the availability of first working silicon.

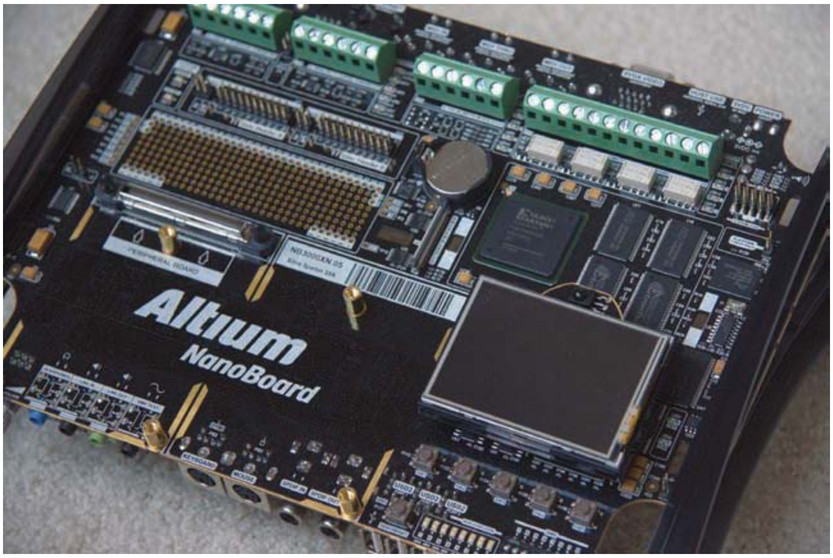


Figure 2 FPGA prototypes usually require more assistance from the user, which may include modification to the RTL, partitioning, mapping, and the design and creation of a board onto which to mount the FPGAs (courtesy Altium).

ware development, debugging, and bring-up were traditionally performed when first silicon came back from the fab, putting it on a critical path. When problems were discovered in the hardware or the software interface, it was usually the software that was expected to change. This situation is no longer acceptable. The earlier that software development can begin, the more likely it is that developers will achieve success. Software requires speed, and silicon and virtual prototypes are the ideal platforms on which to perform this task. However, when detailed visibility into both hardware and software is required—such as when working on device drivers or diagnostics—rapid prototyping provides the necessary features.

Inefficiency and the growing ineffectiveness of constrained random verification techniques have exacerbated the need for verification, a critical-path function for hardware development. This step requires longer and more complex sequences to verify functionality because of both growing system complexity and increasingly large data packets (audio, pictures, low-resolution video, high-definition streaming video over wireless). Abstraction is a key element of speeding the execution of these test cases, but you cannot ignore cycle accuracy for sign-off verification. Further, most hardware developers are becoming system architects. Those developers not working on the implementation of high-value blocks are stitching together IP blocks, making sure that data can move around the system in a timely manner, and looking for ways to reduce power consumption.

PROTOTYPES AVAILABLE

Many development teams plan for more than one chip spin because they may want to provide a platform for software bring-up during hardware optimization. Alternatively, they may be using a previous generation of the chip with some surrounding hardware that enables the addition of new capabilities. They may want to map these capabilities into FPGAs. Typically, a custom board accommodated all of the necessary hardware, ensuring the maximum possible execution speed.

The price of developing this type of prototype includes the board cost. If the prototype uses new silicon, it will be available late in the development cycle, and, in most cases, problems that developers find in software integration cannot influence the hardware. If the developers base the prototype on earlier silicon, it may be available earlier in the development flow so that software can influence the current design. These prototypes are generally the fastest in execution, but they have limited visibility and controllability. When problems are found, they can be difficult to diag-

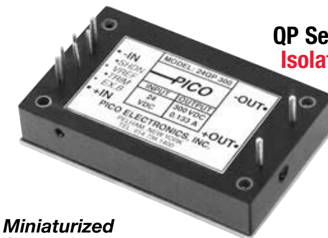


Figure 3 An SDK for an iPhone allows an application developer to write and debug software without executing it on the device.

nose or repeat. The primary developer is the hardware group and may require some unique skills, such as board design. The primary user is the software group. The cost of creating several instances is relatively small and incremental.

Rapid prototyping is the most mature of the group of processes. Hardware, verification, and firmware may use these prototypes, which are cycle-accurate and execute faster than a logic simulator. They coarsely divide into emulation and FPGA prototypes, even though a continuum exists between the categories. Confusion arises because some emulators employ FPGAs, and others don't. To decide between them, you must weigh how much work the user must do versus what tasks the tool flow automates and how much visibility the tool provides into the hardware. Emulators place an RTL design on the hardware with minimal user intervention and provide controllability and visibility similar to that of a simulator. FPGA prototypes usually require more assistance from the user, which may include modification to the RTL, partitioning, mapping, and the design and creation of a board onto which to mount the FPGAs (**Figure 2**). Emulators are more expensive than FPGA prototypes.

The hardware team, initially for its own benefit, usually develops these prototypes. Verification often requires the use of rapid prototypes due to the length of simulation runs. An emulator can turn a multiweek simulation run into minutes, and an FPGA prototype is even faster. However, the emulator still executes at a fraction of real-time speed and is often too slow for software development, except for low-level firmware. Replication cost is high for emulation. FPGA prototypes can be inexpensive if developers use custom boards, but they still cost more than silicon prototypes after amortization of the initial design costs.

Engineers model the emerging family of virtual prototypes at a higher level of abstraction. They are not cycle-accurate because there is no notion of this concept at this stage of design. The prototype need not model all of the functions. The applications for virtual prototypes are software development, hardware-architecture exploration, and verification. An architectural prototype is usually the least complete of the prototypes. In some cases, the prototype models only the bus or the interconnect infrastructure, the memory subsystem, and the generic computation blocks. Traffic generators often feed this prototype to find out how well data moves through the system, to identify bottlenecks that may exist, and to compute throughput requirements for the components. It is rare for this prototype to be used for other purposes.

When high-level synthesis first debuted, it represented an attempt to increase the productivity of the design team. The secondary benefit was an increase in execution speed for verification. The productivity gain of the verification team has been measured to be larger, however, than the gain that the design team experiences. In some companies, the verification team develops the entire prototype and uses it as the comparison model for the hardware. Other teams may then use the same model for software development, and it will remain in sync with the hardware.

Another prototype targets software development, and two variants exist. One can run the same object code as the final target, whereas the second, an SDK (software-development kit), requires recompilation. Developers use SDKs when they do not need to understand anything about the hardware. An example would be an SDK for an iPhone, which allows an application developer to write and debug software without executing it on the device (**Figure 3**). Within the context of chip development, it is more likely for a developer to construct a binary-compatible model, which may also have built-in hardware- and software-debugging capabilities.

The biggest problem today with the construction of virtual prototypes is model availability. Many suppliers of IP do not yet ship abstract models, and, when internal reuse happens, abstract models for those blocks must be created. This step adds to the time and effort necessary to create the prototype.

Almost all emerging design flows employ one or more prototypes, some of which may connect to the hardware-development flow; some, to the verification flow; and some, to software development. Development of these prototypes is key to system-level success, and this success requires a change in team dynamics so that everyone is working toward the same goal. **EDN**


You can reach Contributing Technical Editor Brian Bailey at brian_bailey@acm.org.

BY MATTHEW HANN • TEXAS INSTRUMENTS

Use Spice to analyze DRL in an ECG front end

UNDERSTAND THIS CRITICAL ANALOG FRONT END FOR THIS UBIQUITOUS, VITAL ECG MEDICAL INSTRUMENT.

ECG (electrocardiography) is the science of converting the ionic depolarization of the heart to a measurable electrical signal for analysis. One of the most common challenges in the design of analog electronics interfaces to the electrodes or to patients is optimization of the DRL (driven-right-leg) circuit, which is often added to biological-signal amplifiers to reduce common-mode interference and to increase performance and stability. Using Spice to help in this effort can greatly simplify the process.

In an ECG front end, the DRL amplifier provides a common electrode bias at the reference voltage, V_{REF}, and feeds back the inverted common-mode noise signal, $e_{NOISECM}$, to reduce the overall noise seen at the inputs of the instrumentation amplifier's gain stage. The positive and negative ECG sources, ECG_P and ECG_N, are split to show how the DRL amplifier provides the common reference point for a portion of the ECG signal that is seen at the positive and the negative inputs of the instrumentation amplifier (**Figure 1**).

The parallel RC (resistance/capacitance) combination for the left arm, the right arm, and the right leg represents the lumped passive-electrode connection impedances, which are 52 kΩ and 47 nF. Assuming that e_{NOISE} couples parasitically into the inputs, the feedback of $e_{NOISECM}$ will reduce the overall noise signal at each input, leaving the task of either externally filtering the residual noise or having the CMRR reject the instrumentation amplifier's common-mode noise.

Figures 2, **3**, and **4** show the variation in CMRR of the common-mode test circuit with the varying gain of the DRL amplifier. These plots show that you can achieve the best low-frequency CMRR with no feedback resistor, yielding infinite gain. In reality, however, eliminating the dc path, setting RF to a high value, or using both of these methods may be impractical for applications that require the linear operation

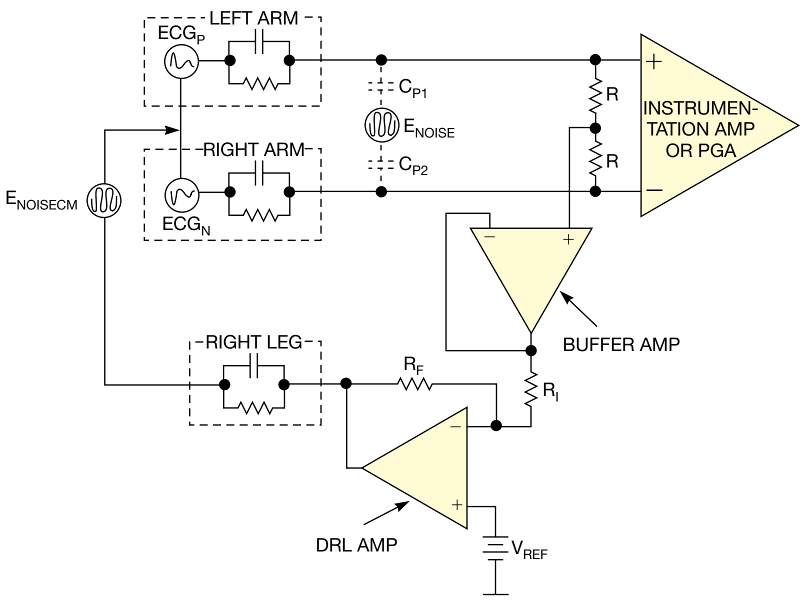


Figure 1 The positive and the negative ECG sources, ECG_P and ECG_N, split to show how the DRL amplifier provides the common reference point for a portion of the ECG signal that the positive and negative inputs of the instrumentation amplifier sees.

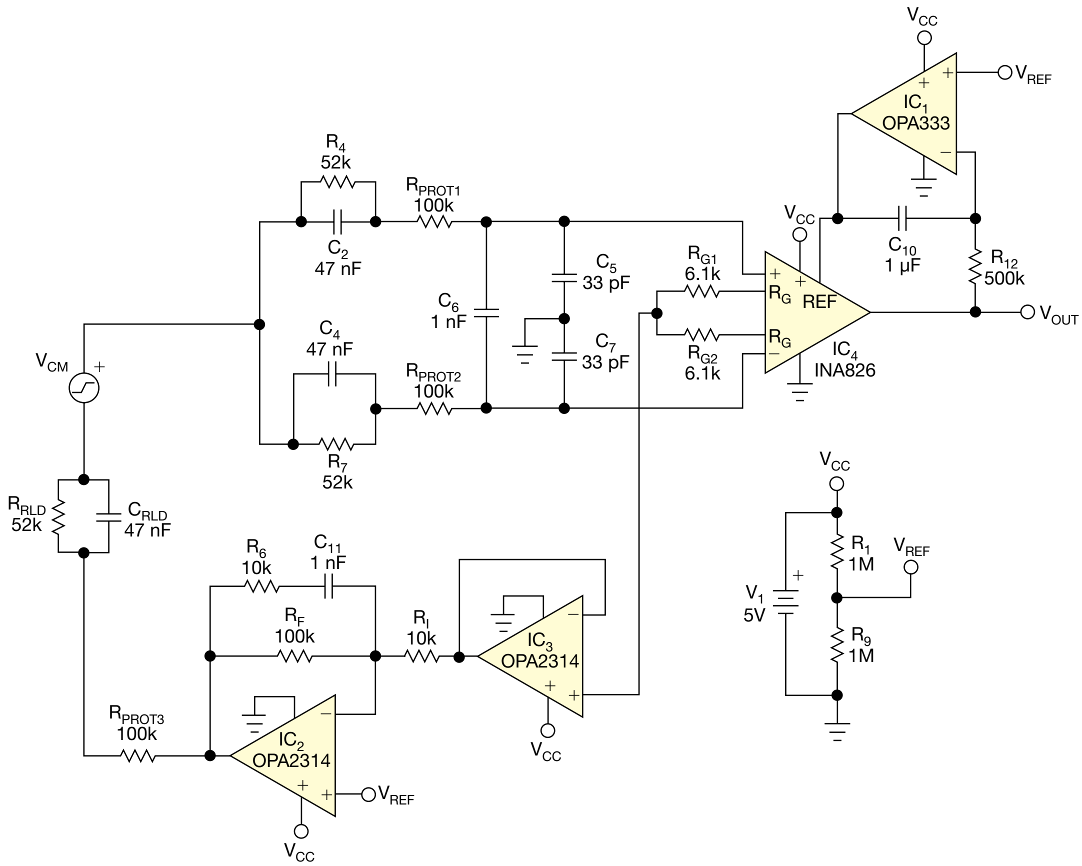


Figure 2 You can achieve the best low-frequency CMRR with no feedback resistor, yielding infinite gain.

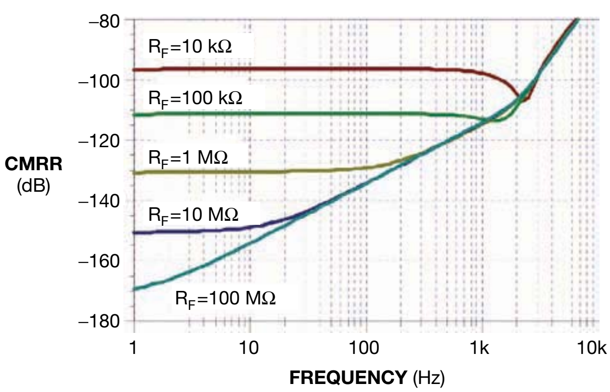


Figure 3 Eliminating the dc path, setting RF to a high value, or using both of these methods may be impractical for applications that require linear operation of the DRL amplifier when you remove one of the input amplifier leads.

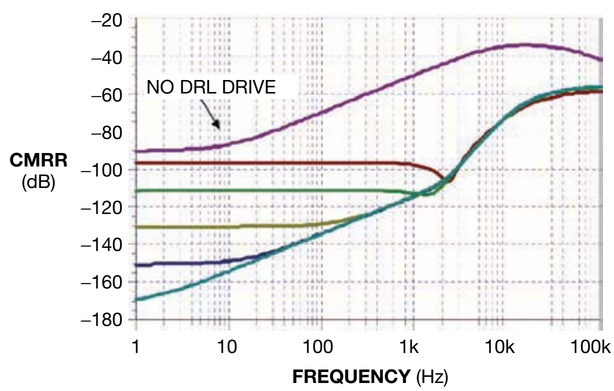


Figure 4 Gain is higher in circuits with no DRL drive.

of the DRL amplifier when one of the input amplifier's leads is removed.

Once you determine the gain of the DRL amplifier, the next step is to inject a small signal step in the loop and monitor the output response (**Figure 5**). In this case, the response shows a strong output oscillation, indicating instability in the loop (**Figure 6**). The dominant feedback path causing this instability is the feedback path for the body, the electrode, and the instrumentation-amp feedback path around the DRL amplifier. A test circuit allows you to separate and analyze the feedback and the open-loop-gain curve of the DRL amplifier on a bode plot (**Figure 7**).

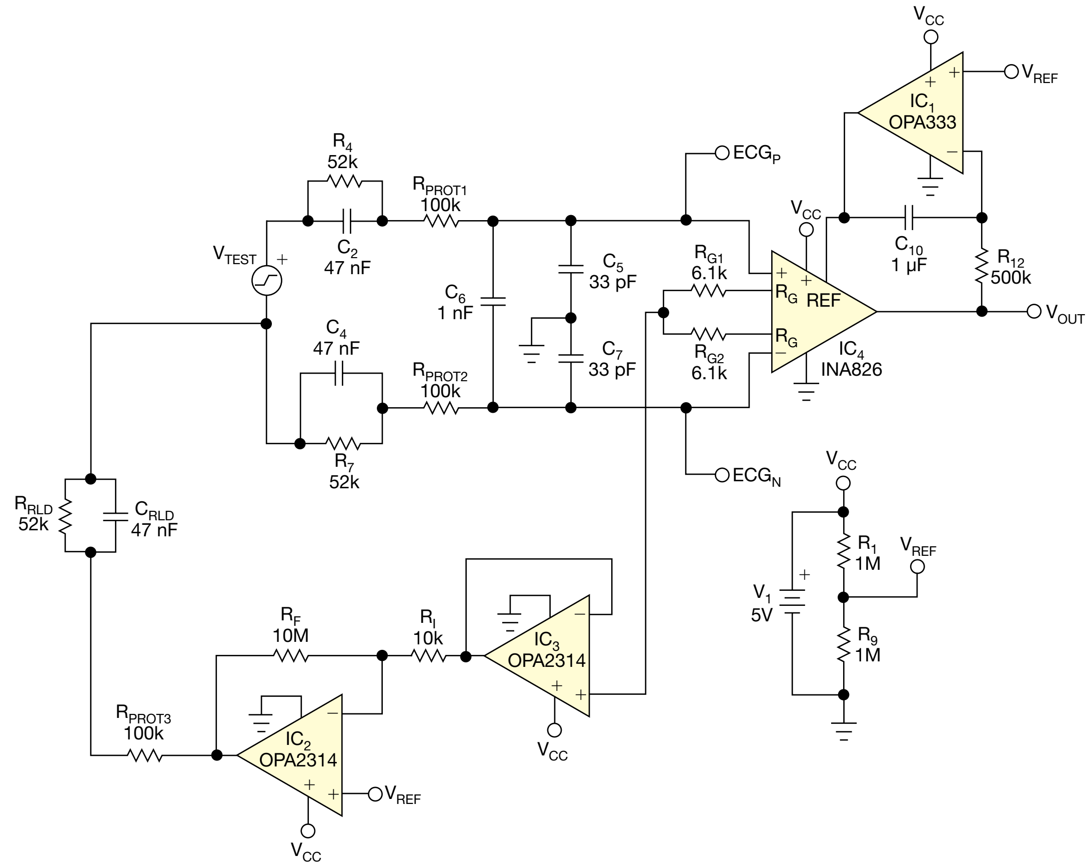


Figure 5 Once you determine the gain of the DRL amplifier, the next step is to inject a small signal step in the loop and monitor the output response.

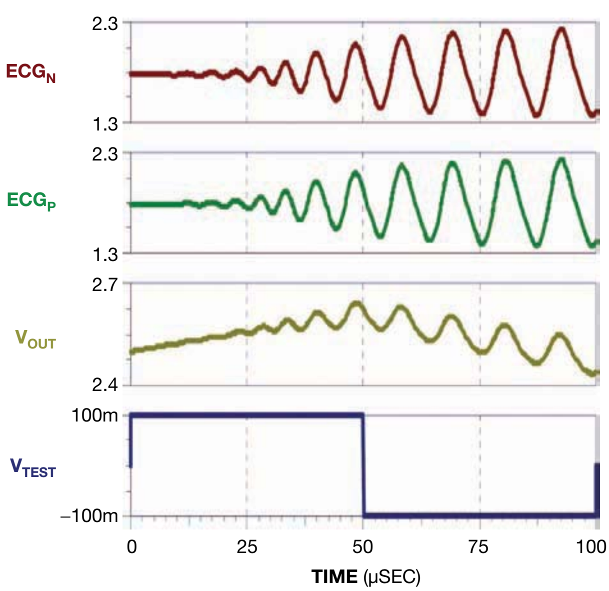


Figure 6 The response shows a strong output oscillation, indicating instability in the loop.

Without an external compensation network, the beta-distribution curve approaches the open-loop-gain curve at a rate of closure greater than 20 dB per decade, indicating instability. To address this issue (**Figure 8**), add series resistor R_C and capacitor C_C (**Figure 9**) in the local feedback of the DRL amplifier. Z_C then becomes the dominant feedback path between 20 and 30 kHz. The result for the simulation in **Figure 7** is represented by the beta (feedback) curve in **Figure 10**. **Figure 11** shows the full circuit of the DRL with compensation. **Figure 12** shows the compensated beta-curve plots, employing variations in R_C and C_C. The overall beta curve intersects the open-loop-gain curve with a rate of closure that is 20 dB per decade or less and a loop gain with a phase margin greater than 45° (**Figure 13**).

Spice can be a useful tool to quickly help analyze and optimize the performance and stability of the DRL's front-end circuitry. Keep in mind that the simulation is only as good as the models, so it is important to correctly model key specifications, such as noise, open-loop gain, open-loop output impedance, and CMRR versus frequency, before analysis and design. **EDN**

ACKNOWLEDGMENT

This article originally appeared on EDN's *sister site*, Planet Analog, *http://bit.ly/uDHbXT*.

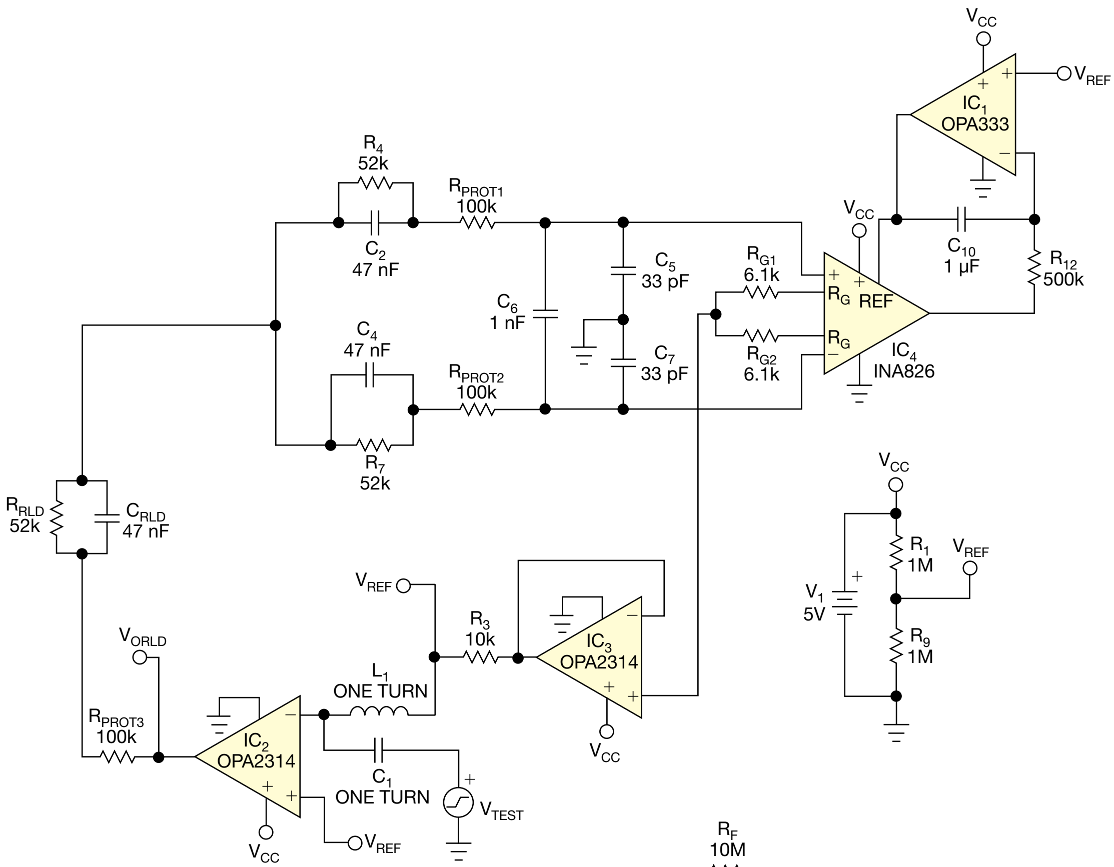


Figure 7 A test circuit allows you to separate and analyze the feedback and the open-loop-gain curve of the DRL amplifier on a bode plot.

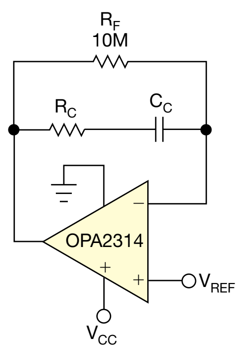


Figure 9 Add series resistor R_C and capacitor C_C in the local feedback of the DRL amplifier.

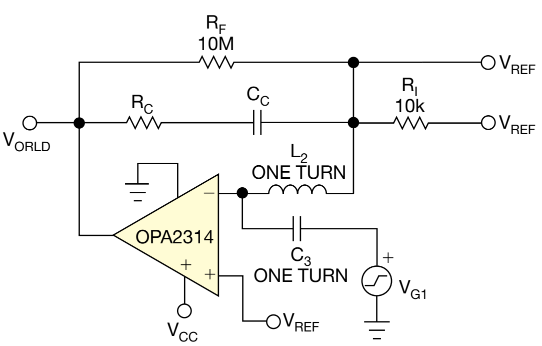


Figure 8 Without an external compensation network, the beta-distribution curve approaches the open-loop-gain curve at a rate of closure greater than 20 dB per decade, indicating instability.

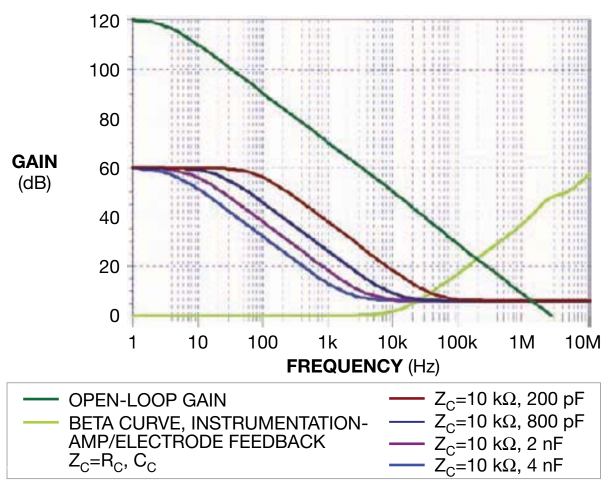


Figure 10 The result for the simulation in Figure 7 is represented by the beta curve.

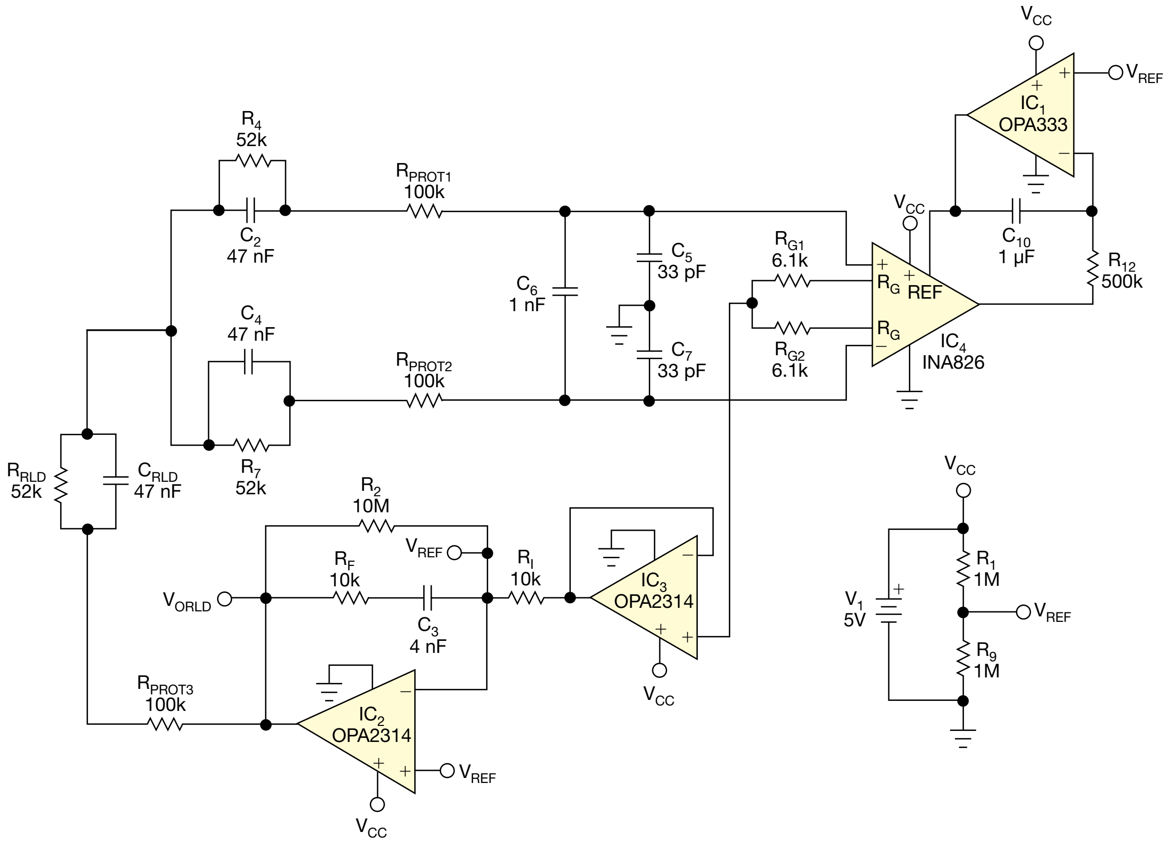


Figure 11 The full circuit of the DRL includes compensation.

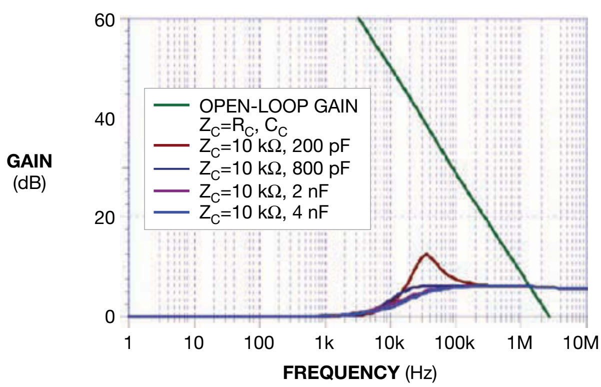


Figure 12 The compensated beta-curve plots employ variations in R_C and C_C.

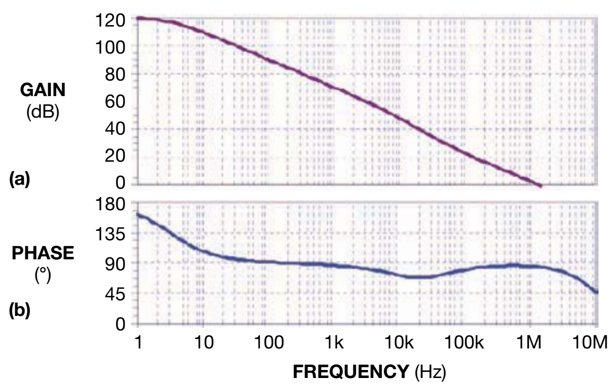
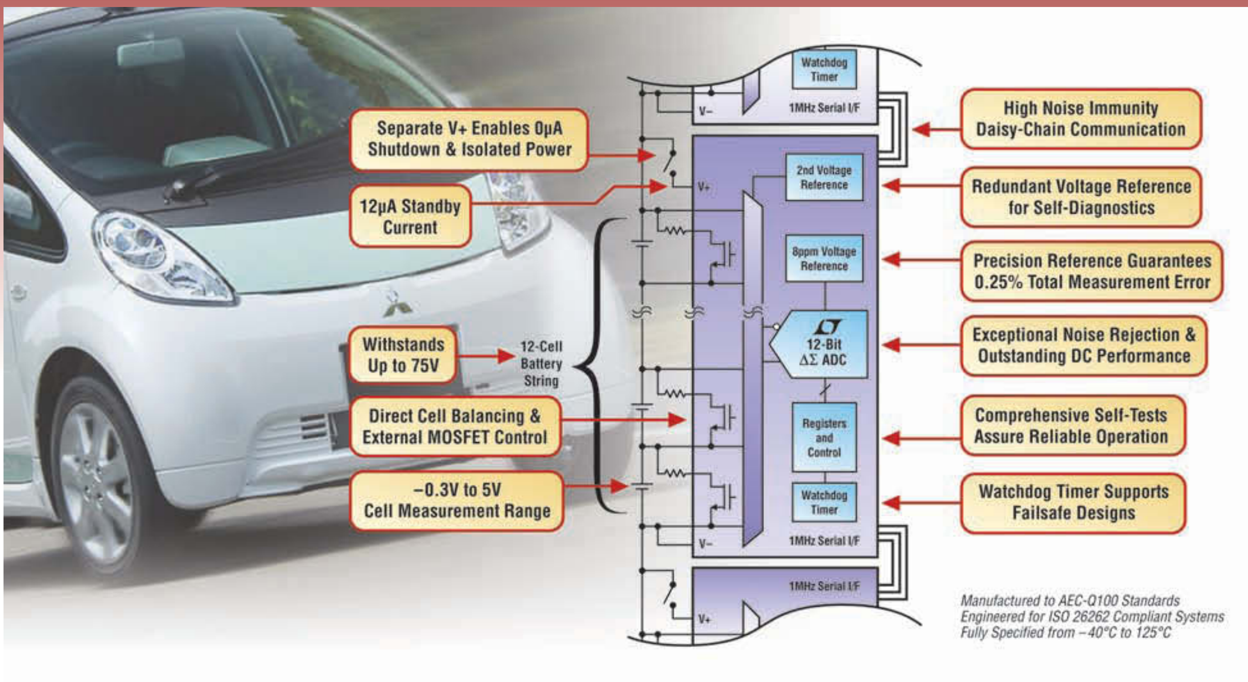


Figure 13 The overall beta curve intersects the open-loop-gain curve with a rate of closure that is 20 dB per decade or less and a loop gain (a) with a phase margin greater than 45° (b).

AUTHOR'S BIOGRAPHY

Matthew William Hann is a precision-analog-applications manager at Texas Instruments. He has more than a decade of product expertise, which includes temperature sensors, difference amplifiers, instrumentation amplifiers, programmable-gain amplifiers, power amplifiers, and TI's line of ECG analog-front-end devices. Through his role as an applications engineer, Hann has developed a focused expertise on the design of analog front ends for medical applications, such as ECGs, electroencephalograms, electromyograms, blood-glucose monitoring, and pulse oximetry. Hann received a bachelor's degree in electrical engineering from the University of Arizona—Tucson. You can reach him at ti_matthann@list.ti.com.

Road Proven Battery Stack Monitor



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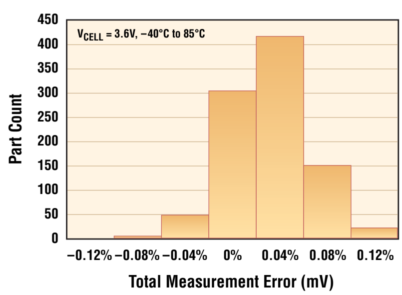

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LINEAR TECHNOLOGY

Use a boost regulator beyond its rated voltage

Kevin Tompsett, Analog Devices, Fort Collins, CO

Inexpensive boost regulators with on-chip FET power switches work well for low-voltage boost converters, SEPICs (single-ended primary-inductance converters), and flyback converters. For higher voltages, designers typically use a more expensive approach comprising a controller with an external FET or a high-voltage boost regulator.

You can instead use an elegant and less expensive approach (**Figure 1**). The circuit uses an ADP1613 step-up dc/dc switching converter to produce a 48V, 100-mA supply, with 86% efficiency at full load (**Figure 2**). The IC includes an on-chip power switch that has 2A peak output currents at 20V. The zener diode acts as a shunt regulator that provides a 5V supply for the IC and biases the gate of the external FET at the same voltage. You connect the internal IC FET in series with a high-voltage FET, a cascode connection. The IC now drives the external FET in a common-gate mode, with the switching voltage at the source of the external FET instead of its gate.

The internal FET then turns on, the V_X node (**Figure 3**) is driven to ground, and the gate of the high-voltage FET remains constant, turning on the high-voltage FET. The lower FET acts like a low-resistance gate driver, and the FET quickly turns on, resulting in low turn-on loss. When the internal FET turns off, the inductor current pulls up the SW node until the external FET turns off. The highest voltage the internal FET will see is the gate voltage minus the threshold voltage of the external FET. The turn-off transition is slower because it is proportional to the peak current in the inductor, but, with a correctly sized FET, there is generally plenty of drive current for a fast transition and low loss, even at low load. The entire BOM cost is less than $2 (1000).

DIs Inside

44 Measure an amplifier's THD without external filters

45 Use air-core-coil resistance to estimate inductance

46 Current monitor uses Hall sensor

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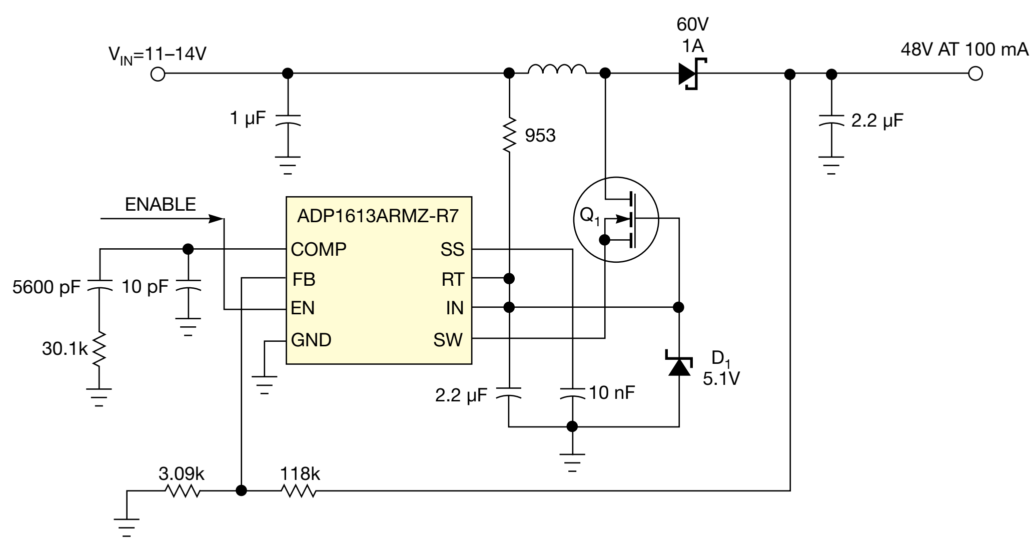


Figure 1 This circuit, designed using ADIsimPower, uses the IC's internal FET switch to drive the source of the external FET.

You can design and simulate this circuit using the ADIsimPower design tool, which is available at www.analog.com/adisimpower. The tool lets you design boost, SEPIC, and SEPIC-Cuk converters using this technique and allows input voltages of 1.8 to 90V and output voltages of 1.2 to 90V. **Figure 4** shows good agreement between the ADIsimPower tool and the measured results, in terms of efficiency. EDN

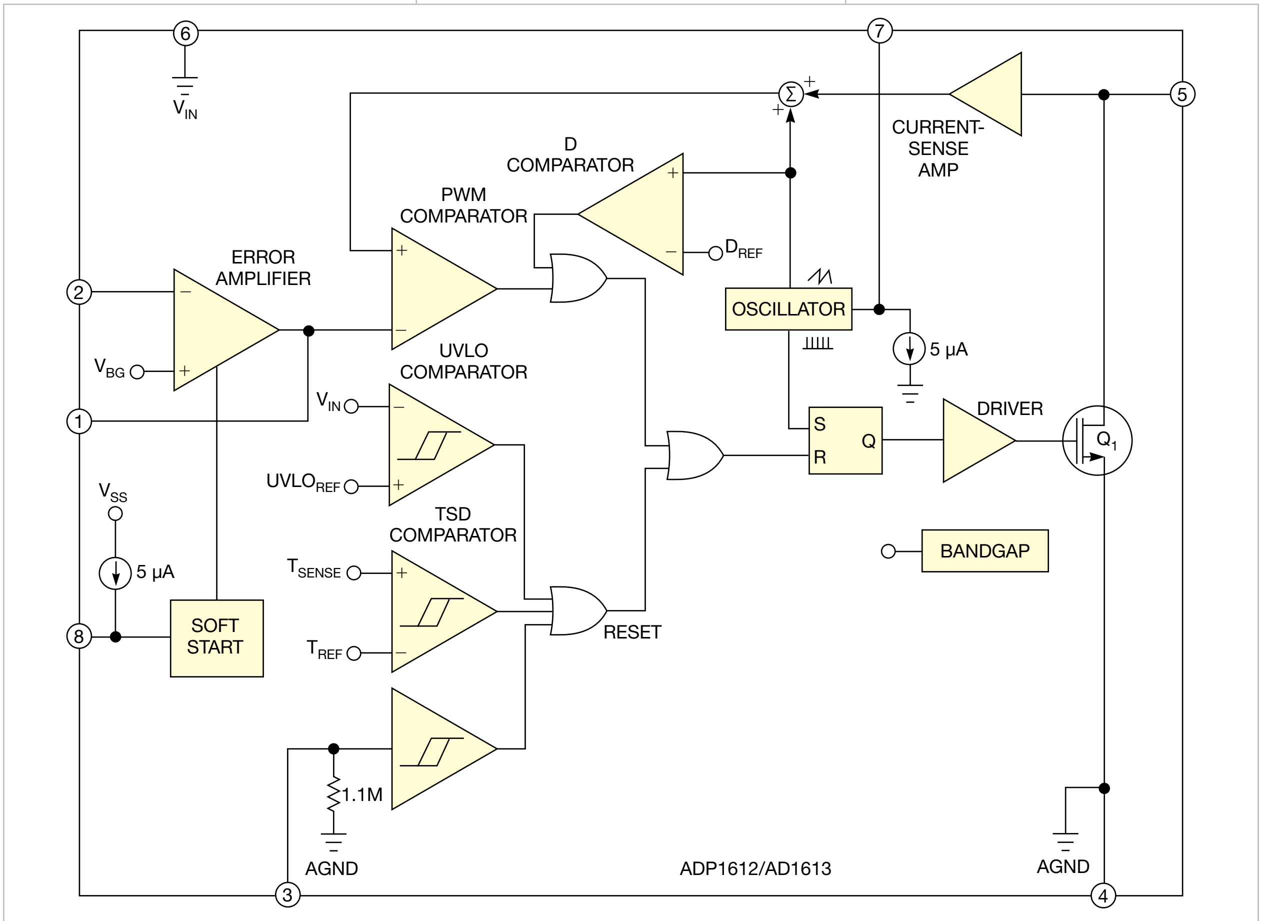


Figure 2 The IC's block diagram shows its boost-converter architecture (courtesy Analog Devices).

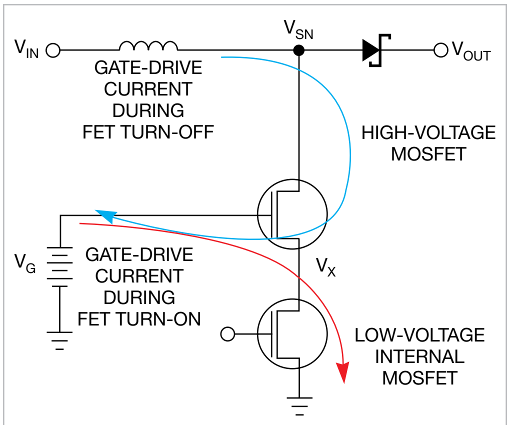


Figure 3 The cascoded-FET arrangement results in fast switch transitions and low loss. The arrangement also enables higher-voltage operation.

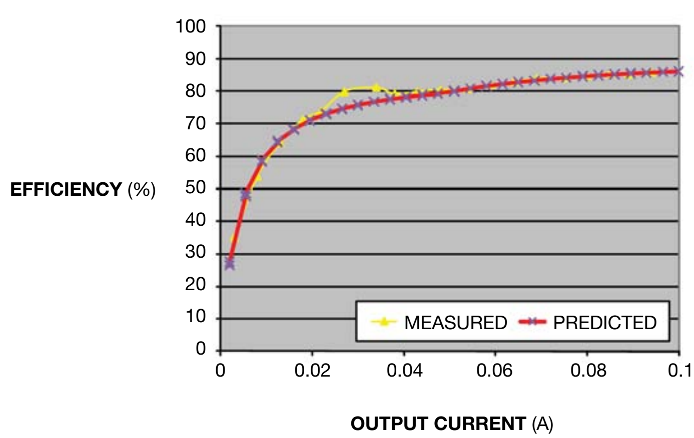


Figure 4 The measured versus ADIsimPower results agree well.

Measure an amplifier's THD without external filters

Ken Mendez, Maxim Integrated Products, Sunnyvale, CA

Measuring an op amp's THD (total harmonic distortion) at frequencies below 100 kHz is problematic because modern amplifiers have a THD rating that is much lower than that of most test equipment. The circuit in this Design Idea uses active noise amplification to eliminate the need for external filters. This approach allows you to measure THD at several orders of magnitude lower than the resolution of the test fixture you are using.

Many THD test circuits use passive-amplification techniques to force the DUT (device under test) to correct itself. This approach can generate considerable error by terminating the distortion signal with resistive loads. A preferred way to generate accurate data is to isolate the DUT and measure it using a high-impedance buffer. This method requires active amplification of the distortion at the amplifier's output. You can use a secondary operational amplifier for active amplification (**Figure 1**). You should use a signal source with THD better than −70 dB. Feed this signal through the DUT, which distorts it. The output of the DUT is a combination of the input signal and the distortion from the DUT multiplied by the gain of the DUT stage. You can set the gain and resistive loading of the DUT according to its specification in the data sheet. This signal at the DUT's negative terminal is the input signal plus the distortion but without any gain. Connect this node to the positive input of the secondary amplifier. You can calculate the output voltage based on the circuit parameters, according to the following **equations**:

$$I_{BUFFER}=\frac{V_{SIG}-(V_{SIG}+V_{DIST})}{100\Omega}.$$

$$V_{OUT}=I_{BUFFER}\times 100\text{ k}\Omega+V_{SIG}=V_{DIST}\times 1000+V_{SIG}.$$

To detect small distortions, set up the secondary amp for a gain of 1000 and connect the amplifier's gain-setting resistor to the input signal. This step allows amplification of the distortion but nulls out secondary amplification of the input signal. Consequently, when referenced to ground, the circuit's output is the original input signal plus the secondary gain times the output distortion of the DUT.

If you want to remove the input signal from the circuit's output, you can set up the secondary amplifier in a differential configuration (**Figure 2**). Some amount of the input signal still reaches the output because of the buffer amplifier circuit's CMRR. However, the signal decreases so that it does not affect the measurement of the amplified distortion. Exact matching of the input and feedback resistors of the secondary amplifier reduces the CMRR effects. Calculate the output of this differential circuit using superposition, according to the following **equations**:

$$V_{OUTTOTAL}=V_{OUTSIG}+V_{OUTSIG+DIST}.$$

$$V_{OUTSIG}=-V_{SIG}\times\frac{100\text{ k}\Omega}{100}.$$

$$V_{OUTSIG+DIST}=\left[V_{SIG+DIST}\times\frac{100\text{ k}\Omega}{100\Omega+100\text{ k}\Omega}\right]\left(1+\frac{100\text{ k}\Omega}{100\Omega}\right)=V_{SIG+DIST}\frac{100\text{ k}\Omega}{100\Omega}.$$

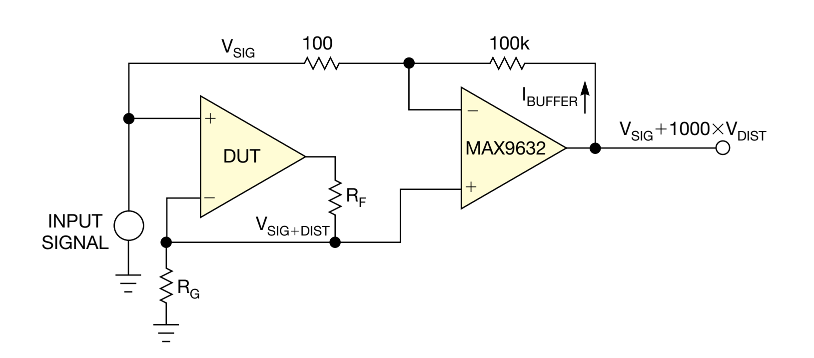


Figure 1 This THD test circuit uses a wideband op amp as a secondary amplifier to allow you to measure distortion.

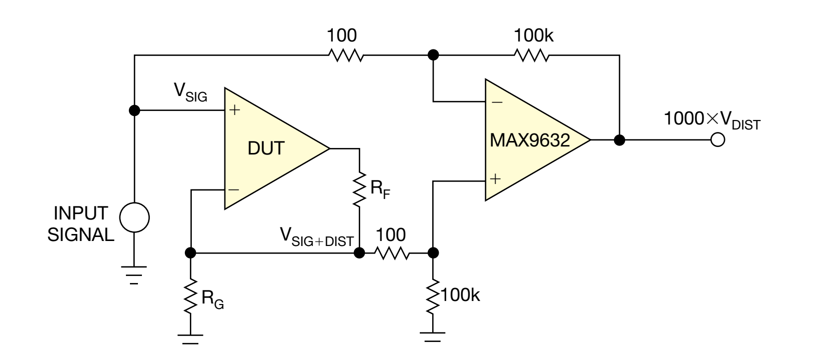


Figure 2 You can set up the secondary amplifier in differential mode to eliminate the input signal from the output.

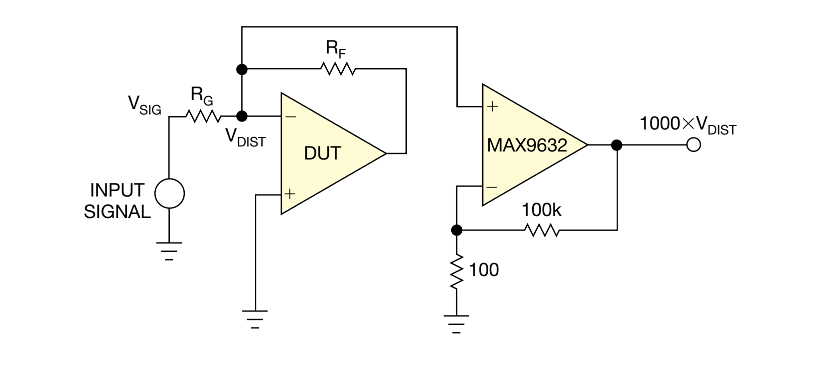


Figure 3 You can modify the circuits in figures 1 and 2 to measure the DUT distortion in inverting mode.

$$V_{OUTTOTAL}=$$

$$V_{SIG+DIST}\frac{100\ k\Omega}{100\Omega}-V_{SIG}\times\frac{100\ k\Omega}{100}=$$

$$V_{DIST}\times 1000.$$

The circuit makes any minor distortion on the input signal irrelevant because it is measuring the difference between the output and the input of the DUT. It removes from the secondary gain stage any distortion on the input. You can modify the setup to accommodate inverting conditions (**Figure 3**). EDN

Use air-core-coil resistance to estimate inductance

Peter Demchenko, Vilnius, Lithuania

This Design Idea shows how to calculate the inductance of a multilayer air-core coil using only its dimensions and resistance. If you know the dimensions and the number of turns on an air-core coil, you can easily calculate the inductance. With the dimensions in millimeters, the inductance, L, in microhenries is a function of the square of the turns, as the following **equation** shows: $L=0.008\times D^2\times N^2/(3D+9h+10g)$, where D is the average diameter of the coil; h is the height of the coil; and g is the depth of the coil—all in millimeters (**Figure 1**).

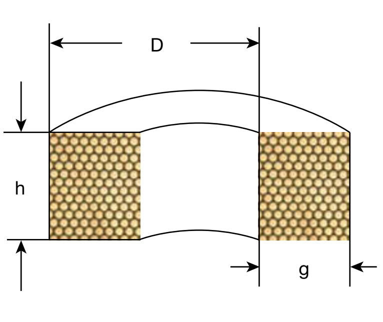


Figure 1 You can calculate the inductance of a coil if you know its dimensions and number of turns.

If you don't know the number of turns, you can still calculate the inductance using the dc resistance of the coil. For this technique to be accurate requires tight and regular coil winding using enameled cylindrical wire (**Figure 2**). You could use the wire dimensions to give an approximate expression for the total number of turns, N: $N=g\times h/d^2$, where d is the diameter of the wire, but this Design Idea assumes that the wire diameter is unknown.

Because the length of an average turn is equal to $\pi\times D$, the total length of the wire is $(N\times\pi\times D)$. The square of the cross-sectional area of the wire is $(\pi\times d^2)/4$.

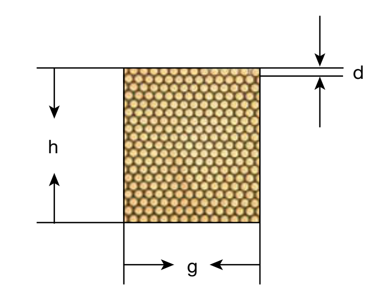


Figure 2 You can estimate the inductance of a tightly and regularly wound coil from its dimensions and resistance.

You can express the resistance, R, of the coil as $R=\rho\times N\times\pi\times D\times 4/(\pi\times d^2\times 1000)=\rho\times N\times D/(250\times d^2)=\rho\times g\times h\times D/(250\times d^2\times d^2)$, where ρ is the wire resistivity in ohmmeters and the resistance is expressed in ohms. Thus, you can derive an expression for the wire's diameter squared: $d^2=\sqrt{(\rho\times g\times h\times D/(250\times R))}$. You would then substitute for the d^2 term in the expression for turns: $N=g\times h/\sqrt{(\rho\times g\times h\times D/(250\times R))}$. You can now square both sides of the **equation** and cancel terms: $N^2=250\times g\times h\times R/(\rho\times D)$. Substituting the value of N^2 into the first **equation** yields $L=2\times D\times g\times h\times R/(\rho\times(3D+9h+10g))$. Using the value of ρ for copper wire, you get an expression for L, which depends only on the resistance and the physical dimensions of the coil: $L=117.7\times D\times g\times h\times R/(3D+9h+10g)$.

L and R are proportional to each other yields, yielding two interesting consequences. First, for a series RLC circuit, the following **equation** defines the damping factor, ζ: $\zeta=R/2\times\sqrt{(C/L)}$, meaning that the damping factor is proportional to the square root of R for a given C and coil dimensions D, g, and h. Second, the quality factor, Q, of a coil with given values of D, g, h, and ρ and an angular frequency of $w=2\pi F$ is a constant value: $Q=wL/R=2\times w\times D\times g\times h/(\rho\times(3D+9h+10g))$. EDN

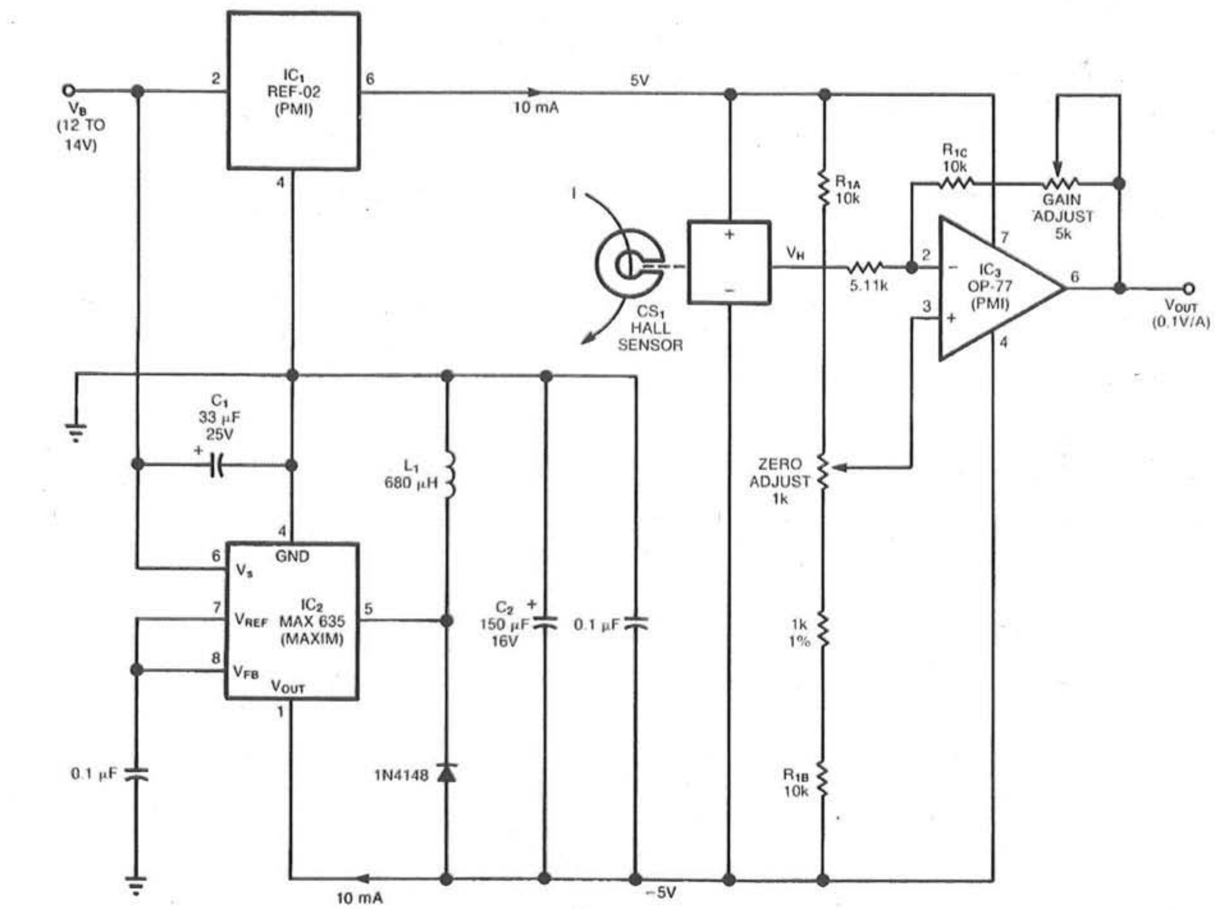
Originally published in the March 31, 1987, issue of *EDN*

Current monitor uses Hall sensor

Paul Galluzzi, Dynamics Research Corp, Wilmington, MA

The **Fig 1** circuit uses a Hall-effect sensor, consisting of an IC that resides in a small gap in a flux-collector toroid, to measure dc current in the range of 0 to 40A. You wrap the current-carrying wire through the toroid; the Hall voltage V_H is then linearly proportional to the current (I). The current drain from V_B is less than 30 mA.

To monitor an automobile alternator's output current, for example, connect the car's battery between the circuit's V_B terminal and ground, and wrap one turn of wire through the toroid. (Or, you could wrap 10 turns—if they'd fit—to measure 1A full scale.) When I=0V, the current sensor's (CS_1's) V_H output equals one-half of its 10V bias voltage. Because regulators IC_1 and IC_2 provide a bipolar bias voltage, V_H and V_{OUT} are zero when I is zero; you can then adjust the output gain and offset to scale V_{OUT} at 1V per 10A. **EDN**



NOTES:
1. C_1 and C_2 ARE 199D TANTALEX CAPACITORS FROM SPRAGUE.
2. L_1 IS A 6860-23 INDUCTOR FROM CADDELL-BURNS.
3. R_{1A}, R_{1B}, AND R_{1C} ARE PART OF A THIN-FILM RESISTOR NETWORK SUCH AS THE CADDOCK T914-10K.
4. CS_1 IS A HALL-EFFECT CURRENT SENSOR (CSLA1CD) FROM MICROSWITCH.

Figure 1 This circuit's Hall-effect current sensor, CS_1, enables V_{OUT} to register dc current at 1V per 10A.

supplychain

LINKING DESIGN AND RESOURCES

Thai flood will affect supply chain in 2012

The flood that took place last year in Thailand will continue to affect this year's electronics supply chain. IHS in December estimated that damages from the flood will result in a 3.8 million-unit shortfall in PC shipments in the first quarter of 2012 compared with the company's previous forecast, which it issued in August. IHS now expects that global PC shipments will grow by 6.8% in 2012, down from the previous outlook of 9.5% growth.

IHS estimates that worldwide PC shipments in the first quarter of 2012 will reach 84.2 million units, down from its earlier forecast of 88 million. The revised forecast calls for an 11.6% sequential decline from 95.3 million units in the fourth quarter of 2011, almost double the typical 6% sequential decline for the first quarter following the holiday season.

The first-quarter reduction has forced IHS to lower estimates for total PC unit shipments in 2012 to 376 million, compared with the company's previous prediction of 399 million. The market-research company says that this result is partly due to a shortage of hard-disk drives, along with weakening demand due to other factors, such as the popularity of tablets. This year's shipments of notebook PCs—a segment that the hard-drive shortage affects and that competes with tablets—should rise by 10.1%, down from the previous forecast of 13.8% growth.

IMAGE: ISTOCKPHOTO

"The PC supply chain says that it has sufficient hard-disk-drive inventory for the fourth quarter of 2011," says Matthew Wilkins, senior principal analyst for compute platforms at the company. "However, those stockpiles will run out in the first quarter of 2012, impacting PC production during that period."

IHS expects the hard-drive supply situation to begin to improve in the first quarter but notes that it will take time to replenish the electronics supply chain. The overall hard-drive supply will meet demand only by the end of the third quarter of 2012. Many drive makers have moved production outside Thailand to supplement supply. PC shipments should rebound from the shortage in the second half of the year. With the added production outside Thailand, the market for hard-disk drives could face an inventory surplus by the end of 2012 after facilities in the country return to full production. **—by Suzanne Deffree**

SOBERING STATS FROM THE SUPPLY CHAIN

Year-end surveys tend to be optimistic or at least to find one silver lining among the clouds. Nobody wants to set a tone of pessimism for the upcoming year. In the wake of reports on the unemployment rate, the European Union's debt management, and the skyrocketing tablet-computer market, however, companies in the electronics supply chain believe that the next few quarters will be tough. VentureOutsource, an EMS/ODM consultancy, in December released a survey that shows a different reality, at least as the electronics supply chain sees it.

On a scale of 1 to 10, with 10 being the most optimistic, the survey's respondents rate their current outlook at an average of 5.34. That figure is down 10% from a survey the company conducted six months ago. The demographics of the report show that 87% of respondents are responsible for participating in purchasing, sales, and operational decision-making. Nearly one in five works in the PC industry. VentureOutsource notes that recent results from companies such as Intel are positive but that smaller companies are reporting mixed results. Overall, the semiconductor segment is seeing revenue growth slowing and layoffs starting to take place. In certain areas, growth prospects are better, but the next several quarters will be challenging for semiconductor companies.

VentureOutsource does not anticipate that semiconductor end-user demand will see sharp uptakes and expects prices in most areas to decline. Few reasons exist for semiconductor decision-makers to be optimistic, except that inventories have already tightened, which means any uptick in demand may prove beneficial to their organizations. EMS/ODM companies, on the other hand, are likely wary of the order volatility they have seen and the worsening end-user demand. With the exception of a few areas, most product segments should see weak demand through 2012.

The report states that developing markets—so far a bright spot for electronics—are now starting to feel the economic pain. China's growth is slowing as both domestic and export markets show weaker demand. To meet these challenges, VentureOutsource notes, EMS/ODM companies have taken steps through the last recession to downsize and remove costs from their operations. Find the full survey at http://bit.ly/tY0MyO.

—by Barbara Jorgensen,
***EBN* Community Editor**

This article was originally published by EBN: *http://bit.ly/vZJoCl.*

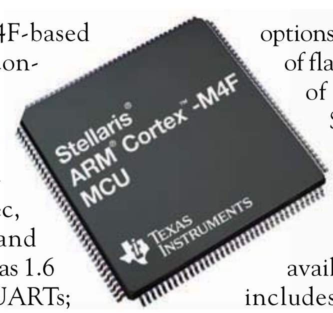
productroundup

MICROCONTROLLERS

Microchip's PIC32 MX1 and MX2 microcontrollers operate at 105°C

Operating at 105°C, the PIC32 MX1 and MX2 microcontrollers include as much as 32 kbytes of flash memory and 8 kbytes of SRAM, two I^2S interfaces for audio processing, the vendor's CTMU (charge-time-measurement-unit) peripheral for adding mTouch capacitive-touch buttons or advanced sensors, and an 8-bit parallel-master-port interface for graphics or external memory. The devices also feature an on-chip, 10-bit, 1M-sample/sec, 13-channel ADC, as well as USB 2.0 and serial-communications peripherals. Prices start at $1.58 (10,000).
Microchip Technology Inc, www.microchip.com

TI's Stellaris uses ARM Cortex-M4F



The Cortex-M4F-based Stellaris microcontroller includes a floating-point core operating as fast as 80 MHz, two 12-bit ADCs sampling at 1M sample/sec, three comparators, and standby currents as low as 1.6 µA. The unit supports UARTs; host, device, and OTG USB; I^2C; SSI/SPI; and CAN. Other features include integrated EEPROM and options for as much as 256 kbytes of flash memory and 32 kbytes of SRAM. Prices start at $1.53 (10,000). The EK-LM4F232 evaluation kit is available for $149. Royalty-free StellarisWare software is available for free download. It includes hundreds of example projects, application and peripheral libraries, and open-source stacks.
Texas Instruments, www.ti.com

Atmel expands 32-bit AVR UC3 portfolio

The AVR UC3L, D, and A4 microcontrollers feature DSP instructions, USB connectivity, secure encryption, and capacitive-touch support. The UC3L consumes 165 µA/MHz in active mode, as little as 600 nA with the RTC running, and as little as 9 nA in deep-sleep mode. The devices have 128 or 256 kbytes of flash memory and 32 kbytes of internal SRAM. The UC3D features a RTC with calendar; a 10-bit ADC; and USART, SPI, TWI, PWM, and I^2S interfaces. You can use a peripheral to wake the device from sleep mode using proximity touch. The UC3D supports as many as 25 channels in hardware. The UC3A4 targets use in PC peripherals, e-tokens, high-speed communication, audio, and other applications requiring security. It features performance of 1.51 DMIPS/MHz, 128 kbytes of onboard SRAM, and onboard high-speed USB OTG. The UC3L0 and UC3L4 come in 48-pin QFN packages and TQFPs. Prices start at $2292 for quantities of

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10,000. Prices for the UC3A4 and UC3D start at $4208 and $2945, respectively, for quantities of 10,000.
Atmel Corp, www.atmel.com

NXP's LPC11D00 and LPC12D00 integrate segment-LCD drivers

The Cortex-M0-based LPC11D00 and LPC12D00 microcontrollers integrate LCD drivers, enabling high contrast and brightness. Featuring the vendor's PCF8576D LCD driver, the units can drive any static or multiplexed LCDs containing as many as four backplanes and 40 segments. Designers can easily cascade these LCD drivers to accommodate as many as 2560 segments. The PCF8576D LCD driver supports a supply range of 2.5 to 6.5V, making the microcontrollers suitable for use in interfacing with both low- and high-threshold LCDs. The LPC11D00 supports as much as 32 kbytes of flash memory; 8 kbytes of SRAM; an I^2C interface; UART; four system timers; and an eight-channel, 10-bit ADC. The LPC12D00 has as much as 128 kbytes of flash memory, dual analog comparators with 32 levels of voltage reference, edge and level detection, and output-feedback loop. The LPC11D00 and LPC12D00 sell for $1.53 and $2.19 (10,000), respectively.
NXP Semiconductors NV, www.nxp.com

Freescale K70 enriches human-machine-interface applications

The Cortex-M4-based Kinetis K70 microcontroller targets applications that require a sophisticated graphics-LCD user interface, advanced connectivity, and security. The PEG (portable embedded graphical user interface) supports the family, providing a comprehensive visual-layout and -design tool that accelerates design by allowing developers to create GUIs with simple PC-based environments. The 120- and 150-MHz K70 microcontrollers add new features to the K10, K20, and K60 families. These features include a floating-point unit that extends the range of data-acquisition-intensive applications, such as motor drive, audio processing, and digital filtering, by reducing computation time and increasing accuracy. The devices also feature high-speed USB OTG supporting 480-Mbps data transfer. DRAM and NAND-flash controllers enable the connection of DDR, DDR2, and low-power DDR memories and 32-bit NAND memories. The 120-MHz Kinetis K70 microcontroller with as much as 1 Mbyte of flash memory comes in a 256-ball MAPBGA package and sells for $10.09 (10,000).
Freescale Semiconductor, www.freescale.com

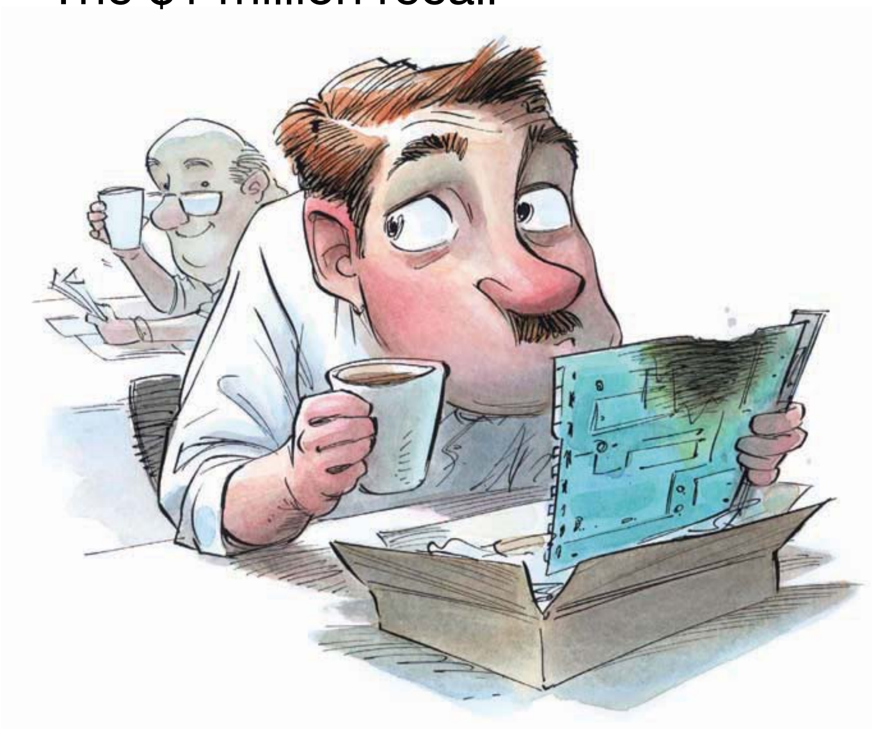
Energy Micro adds more than 100 EFM32 microcontrollers

The Leopard Gecko EFM32 microcontroller family offers 64, 128, or 256 kbytes of flash memory, and high-end Giant Gecko devices offer 512 or 1024 kbytes of flash memory with 128 kbytes of RAM. The CPUs operate at speeds as high as 48 MHz, and a 400-nA backup-power mode enables the real-time clock to keep running and provide 512 backup register bytes, protecting against clock reset and data loss during a momentary power loss. The devices integrate three on-chip op amps and an 8×36-segment LCD controller. They provide the option of a 320×240-dot, direct-drive TFT controller that can drive display updates without CPU intervention. EFM32 Gecko microcontrollers can achieve an active-mode current consumption of 160 μA/MHz and provide a deep-sleep mode, with the real-time clock running, that consumes 400 nA; a shutoff mode, with general-purpose-I/O wake-up, consuming 20 nA; and wake-up from sleep modes as short as 2 μsec. The EFM32 Leopard Gecko and Giant Gecko sell for $2.47 and $3.53 (100,000), respectively.
Energy Micro AS, www.energymicro.com

Fujitsu adds two-channel Ethernet-MAC support to FM3 family

The Cortex-M3-based FM3 family of 32-bit RISC microcontrollers includes the MB9B610, 410, 310, 210, and 110 series and the MB9A130 series. The MB9B family operates at clock speeds as high as 144 MHz and supports as much as 1 Mbyte of high-speed flash memory and 128 kbytes of RAM, a one- or two-channel Ethernet MAC, USB 2.0 host and slave functions, CAN, and inverter-control timers with as many as three channels. They come in 176- and 144-pin LQFPs and 192-ball BGA packages. Prices start at $7.88 (small volumes). The low-leakage MB9A130 family supports voltages of 1.8 to 5.5V and draws 1.6 μA when using real-time-clock mode under date and time management and 1.2 μA in deep-standby mode using the real-time clock. The device is available in 48- to 64-pin packages with 64 to 128 kbytes of flash memory and as much as 8 kbytes of RAM. Prices start at $2.18.
Fujitsu Semiconductor America Inc, www.fujitsu.com

The $1 million recall



DANIEL VASCONCELLOS

This story began in 2003 when a 1000W power module, which just a day before was part of a huge optical-telecom network, came back from the field heavily burned, interrupting a network that transmitted many gigabits per second. The issue immediately hit the radar of the highest management. I delved into a world of telecom power modules, which "must" work forever. To achieve forever, the power distribution is made redundant: Although one unit can do the job, two power modules power the same rack in case one fails and needs replacement, which would be performed by so-called hot-plugging while the rack is under power.

Hot-plugging a power module into a 40 to 60V telecom bus is tricky. The current flow to the module is controlled by an onboard MOSFET; to deal with 1 kW, it must be fully on or fully off. Upon module insertion, the transition from off to on must be fast but not too fast; otherwise, the inrush current may brown out the telecom bus.

Prior to deployment, the power module passed the insertion test, but the dreadful short test had not been comprehensively tried. It turned out that the delayed reaction blew the MOSFET short. In the field, one of the module's capacitors failed short, and the MOSFET followed, allowing hundreds of amperes to enter the board. After a few seconds, the hub was full of smoke, and the main circuit breaker tripped.

The fix was to redo the hot-swap timing, which was set by a few resistors and capacitors. As mundane as the job of calculating their values may sound, it was a vital task. The demonstration of the power module shutting down and restarting in a controllable manner during various induced shorts vindicated the efforts.

The company had deployed more than 1000 of these modules. The fix would cost $10 for parts, and more than $1 million to recall, modify, and redeploy the units. The verdict from upper management: Proceed with the fix. I appreciated the trust.

Three years later, I received an e-mail informing me that a power module had come in from the field with possible telemetry failure. The telemetry had stopped weeks earlier, but the hub was operating flawlessly, so the service visit was delayed. The replaced unit looked innocent when it arrived but smoked immediately in a test rack. I knew in my gut that this unit was modified.

I ran into the lab to look at the power module. During the dash, I thought about whether it was appropriate to compensate my company for the wasted $1 million. The thought of monetary loss sharpened my senses. Upon arrival, I focused my attention on the laboratory power supply connected to the test rack with a visibly smoked module. Now, guided by brain rather than gut, I checked the laboratory supply's setting. Eureka! The current limit on this supply was set to 18A; reaching this level would turn this supply into a *current* source.

After I stopped worrying about my savings, I started to think coherently. All of the deployed power modules had MOSFET circuit breakers set to 30A, with a 20% margin for 1 kW at 40V. Under lab conditions of 50V and 20°C, the test rack consistently demonstrated consumption of approximately 800W. Subsequently, the lab supply's limit was set to 18A. I guessed there would be a short on the returned module, but the external 18A limit didn't allow the module to recognize the supplied current as a short. Upon power-up, the MOSFET was kept in linear mode until its demise.

For weeks, thanks to redundancy, one module kept the rack operational, while the shorted module, with access to unlimited power, reacted happily to 30A inrush current, keeping the MOSFET alive by kicking on and then immediately off every few seconds. The overprotective lab settings killed the MOSFET in 20 msec. I still wonder whether a penny capacitor was the culprit. EDN

Congratulations to Samuel Kerem, author of this entry and winner of *EDN*'s Tales From The Cube: Tell Us Your Tale contest, sponsored by Tektronix. Kerem will receive a Tektronix scope valued at approximately $5000. Read the other finalists' entries at http://bit.ly/Talesfinal_EDN.

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